Contents

Experiment No.1

FET CHARACTERISTICS

Aim :-

To study the static output and transfer characteristics of a FET (Field Effect Transistor) and to determine the drain resistance, Trans conductance, and amplification factor.

Apparatus:-

Field effect transistor(BFW10), 0-30V (with voltage and current indication),100mA variable DC voltage power supply, potentiometers (0- 1Mohms,0-10 k ohms, and D.C milliammeters (0-50 mA, 0-1mA), Volt meters (0- 50 Volts, 0-5V).

Theory:

FET is a three terminal device. FET's can be characterized in two main categories like JFET(Junction Field Effect Transistor) and MOSFET(Metal Oxide Field semiconductor). Here we study the JFET characteristics. JFET's are further of two types n-channel type and p-channel type.

Main feature of JFET:-

1. It is a uni-polar three terminal device, which solely depends on the conduction of either of electrons or holes.
2. In the operation of this the electric field established by the charges controls the conduction; hence the name Field Effect Transistor.
3. Field Effect Transistor is a voltage control device where as BJT is a current control device. The output current in the BJT is controlled by the input current level where as the output current in FET is controlled by the applied voltage in the input circuit.
4. There are two types of BJT i.e p-n-p and n-p-n. Similarly FET is of two types p-channel FET and n-channel FET.
5. Gate-source junction is generally reverse biased and gate drain junction is forward biased.
6. The effective channel width, which allows current flow, is controlled by reverse biasing the gate source junction, which changes the width of the space charge in the channel.
7. The reverse bias voltage given to gate- source junction, which just prevents the current flow from the source to drain is called "pinch off voltage".
8. By increasing the drain voltage, drain current increases. At some value of V_D breakdown occurs. Then an avalanche current will flow which is very large. This is called breakdown region.

Parameters of FET:-

1. Dynamic Drain resistance (r_d):-

Dynamic drain resistance at an operating point is defined as the ratio of small change in drain voltage to the corresponding change in the drain current , when the gate voltage is kept constant.

$$r_d = (\Delta V_{DS}) / (\Delta I_D) \quad V_{GS} \text{ being constant.}$$

The typical value of r_d is 200Ω(ohms).

2. Mutual Conductance or Trans conductance (g_m):- The trans- conductance at an operating point is defined as the ratio of a small change in drain current to the corresponding change in gate voltage when drain voltage is kept constant.

$$g_m = (\Delta I_D) / (\Delta V_{GS}) \text{ when } V_{DS} \text{ is constant.}$$

Typical value of g_m is 12mho

3. Amplification Factor (μ):- Amplification factor is defined as the ratio of small change in drain voltage to the corresponding change in gate voltage when drain current is kept constant.

$$\mu = (\Delta V_{DS}) / (\Delta V_{GS}) \text{ when I is constant.}$$

μ being the ratio of two voltages it has no units. Typical value of amplification factor of FET is around 1. The above parameters are related by

$$\mu = (r_d) \times g_m$$

Construction:-

n-channel type JFET starts with n type silicon bar. The two ends of it with attached ohmic constants behave like two terminals called source and drain. Heavily doped p type regions are diffused in to it on either side called gates (see FIG 1). Generally the two gates are connected together.

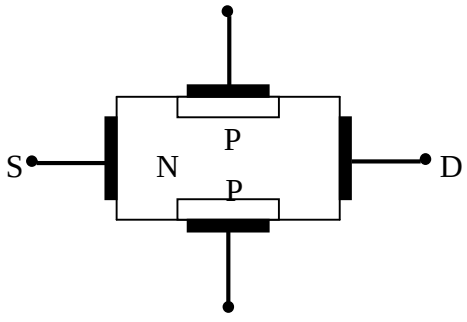


Fig:1

An alternative method of preparation is also there (see FIG 2). A lightly doped n type semiconductor is doped into the p type material, which serves as the channel, and further a heavily doped p type material is doped in to the n type material as shown (see FIG 2).

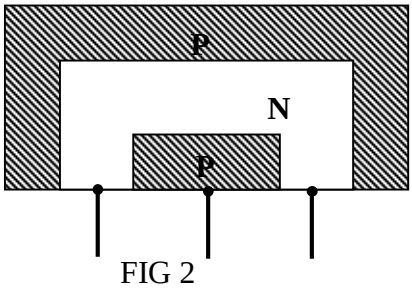


FIG 2

The drain and the source terminals are taken from n-channel and gate terminal is taken from p type material.

Schematic representation:-

Fig 3shows the schematic representation of FET

(a) (b)

FIG 3

The arrow mark on the gate terminal indicates the direction in which gate current flows when gate junction is forward biased. For n-channel FET arrow is shown is shown into the gate.
For p- channel FET away from gate.

Source:- It is the terminal through majority charge carriers enter the bar.

Drain:- It is the terminal through which majority charge carriers leave the bar.

Gate:- It is the terminal which analogous to base terminal in BJT(Bipolar Junction Transistor) and controls the flow of charge carriers.

Channel:- The region between the source and drain through which majority charge carriers move. The width of this is adjustable by controlling the space charge region in it.

Procedure:-

The connections are made as shown in the circuit diagram (see FIG 4)

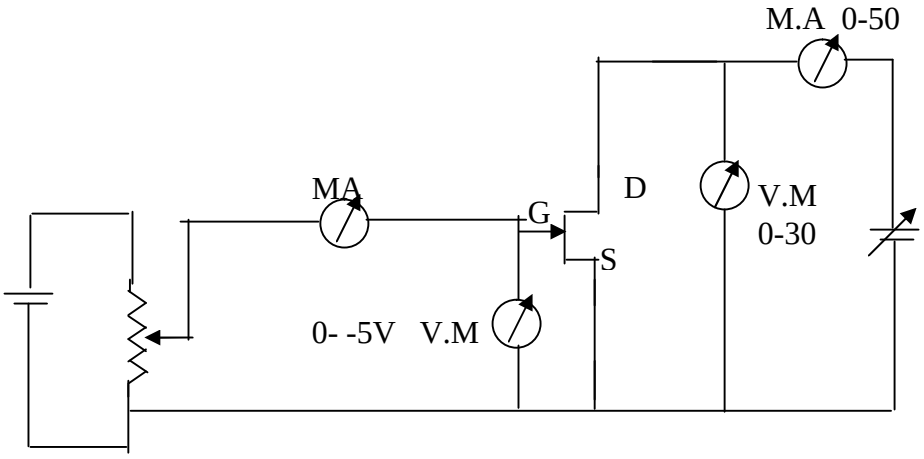


Fig 4

To draw the o/p characteristics :

V_{GS} is kept initially at zero voltage. V_{DS} is varied and the corresponding values of the I_D are noted. Next V_{GS} is kept at -1V, -2V, …… and then for each value of $V_{GS,}$ the values of I_D corresponding to different value of V_{DS} are noted. These observations are recorded in the tabular form. A graph is plotted between V_{DS} and I_D showing the variation of I_D with

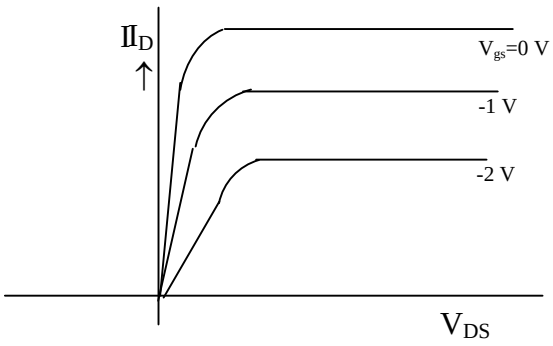


Fig 5(a)

V_{DS}. Different curves are obtained corresponding to different values of V_{DS} . Those are called output characteristics (see FIG 5a).

To draw the transfer characteristics:-

Keeping the value of V_{DS} constant, varying the (negative) gate voltage in steps the corresponding values of the output current I_D are noted. This procedure is repeated for different values of V_{DS}. Graph is plotted taking V_{GS} on the –ve X-axis and I_D on Y-axis (see FIG 5b).

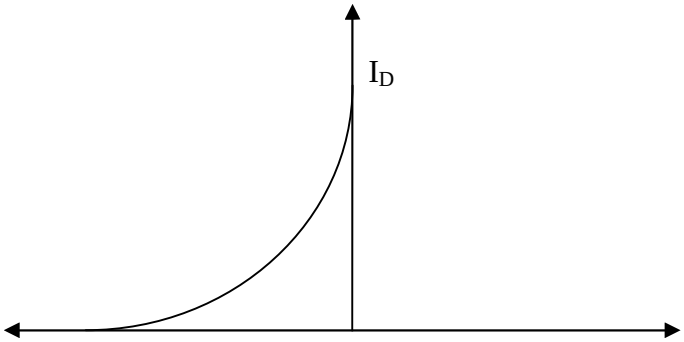


Fig.5(b)

Observations are recorded in the following tabular forms:
Output characteristics: -

$V_{GS=0V}$		$V_{GS=-1V}$		$V_{GS=-2V}$	
V_{DS} (volts)	I_D(mA)	V_{DS} (volts)	I_D (mA)	V_{DS} (volts)	I_D (mA)

From the output characteristics r_d and μ are determined by taking the ratios $(V_2-V_1)/(I_{d2}-I_{d1})$ And $(V_{d2}-V_{d1})/(V_{g2}-V_{g1})$

Transfer characteristics:-

$V_{DS=}4V$

V_{GS} (volts)	I_D (mA)

Transconductance is determined from the graph from the ratio $(I_{d2}-I_{d1})/(V_{g2}-V_{g1})$

Amplification factor of the FET is determined from the relation $\mu = r_d g_m$

Typical values for BFW 10 are r_d= 200Ω; g_m =12 mho; μ = 1

Precautions

1. Before making connections the terminals of the FET are to be correctly identified.
2. Dry soldering is to be avoided.
3. Gate terminal should not be forward biased.

4. The maximum voltage at the gate should not be more than five volts
5. The maximum drain to source voltage for each gate voltage should not exceed breakdown voltage.
6. Leads of FET should not be touched with hands without proper grounding
7. Current meters must be connected at a point (in series) and voltmeters across any two points of interest following polarity.

Result:

The output and transfer characteristics of a FET are studied and the drain resistance, trans conductance and amplification factor are determined to be

Trans conductance =

Amplification factor =

Drain resistance =

Experiment No. 2

UJT CHARACTERISTICS

Aim: To study I –V characteristics of the unijunction transistor (UJT) and to find the intrinsic stand – off ratio (η)

Apparatus:

UJT 2N 2646	1
Resistors 2.2kΩ	1
100kΩ	1
Regulated power supply (0 –20 V)	1
Ammeter (0 – 50mA)	1

Theory:

UJT is a three terminal device but it has a single p-n junction hence the name uni junction transistor. It was originally called duo (double) base diode due to the presence of two base contacts. The main difference in the construction of the UJT and that of the FET is that the emitter junction of the former is much smaller than the gate surface of the latter. The FET is always operated with the gate junction reverse biased, where as the UJT is operated with emitter junction forward-biased. The resistance between base1 and base2 is called the inter base resistance, and lies in the range 5k to10k Ohms.

Equivalent circuit of UJT:

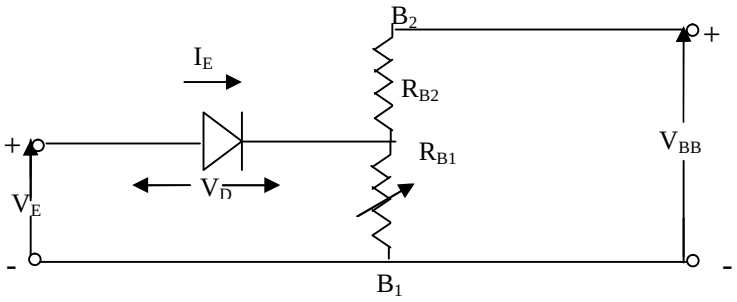


Fig.1 UJT: equivalent circuit

Here R_{B1} and R_{B2} represent the resistances of silicon bar R_{B1} is shown variable as it varies with the current $I_{E.}$ When emitter is kept open then the voltage V_1 is that which appears across R_{B1} due to potential division of V_{BB}. Inter base resistance is that between B_1 and B_2 when I_E =0.

$V_1 = V_{RB1}=[R_{B1}/(R_{B1}+R_{B2})].V_{BB}$

$= \eta.V_{BB}$ Where η is called stand of ratio.

η==$[R_{B1}/(R_{B1}+R_{B2})]$. Where I_E=0, Typical value of η is 0.5 to 0.8.

Let the junction voltage be 0.6(V_B) hence the emitter junction remains reverse biased till V_E is below (V1+V_D) Once V_E exceeds (V_1+V_D) the PN junction gets forward biased then holes get injected into the silicon bar and the resistance between E and B_1 get reduced giving negative resistance effect and the emitter current increases causing V_1 to fall. This static emitter characteristic is as shown in FIG 2.

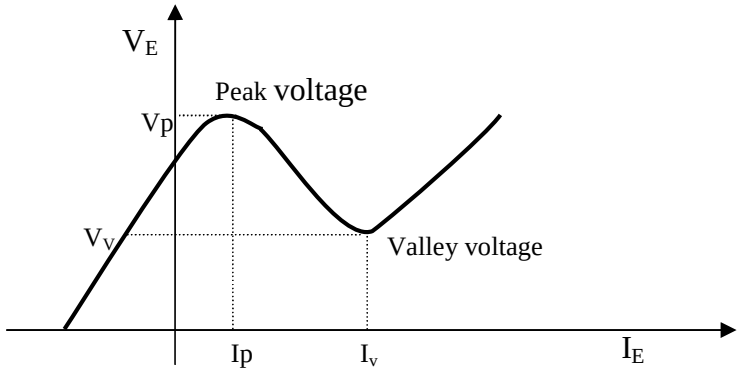


Fig2: UJT emitter characteristics

The peak voltage at which the junction gets which forward biased V_p=V_D+V_1.
Hence V_{RB1}=V_p-V_D , V_p can be obtained from graph.
$V_D$depends on the junction (nearly equal to 0.6) Hence $\eta = V_1/V_{BB}$
$=(Vp-V_D)/V_{BB}$

where,

η = intrinsic stand-off ratio
V_p = peak point voltage
V_B = emitter junction voltage drop = 0.7v
V_{BB} = inter base voltage.

Thus stand of ratio η can be calculated.

Main features of UJT:

1. Useful behavior of UJT occurs when the emitter junction is forward biased. A difference can be noticed by comparing this with the operation of JFET where gate is normally operated by reverse biasing.
2. This is a low power-absorbing device and thus becomes a choice in the design of circuits of relatively high efficiency.
3. It has a large number of applications – oscillators, trigger circuits, saw tooth generator, voltage and current regulator, and power supply.
4. UJT is preferred in construction of relaxation oscillator, which can be used to trigger silicon-controlled rectifier.

Construction: A lightly doped n-type silicon bar (high resistance) has two ohmic contact terminals at the two ends of it. Those two terminals are called base 1 and base 2. An aluminum wire which forms emitter terminal is alloyed to silicon bar on the other surface of the bar at a point closer to base 2 terminal than the base 1 terminal. Base 2 is made positive with respect to base1 terminal. Aluminum wire alloyed to silicon bar forms the p-n junction.
The arrow mark indicates the direction of conventional current (flow of holes) when device is forward biased (see Fig 3) The two base terminals are on either side of the emitter terminal. Base 2 is that terminal which is to be connected to higher potential and is closer to the extension lip of the casing.

Procedure: The connections are made as shown in circuit diagram.

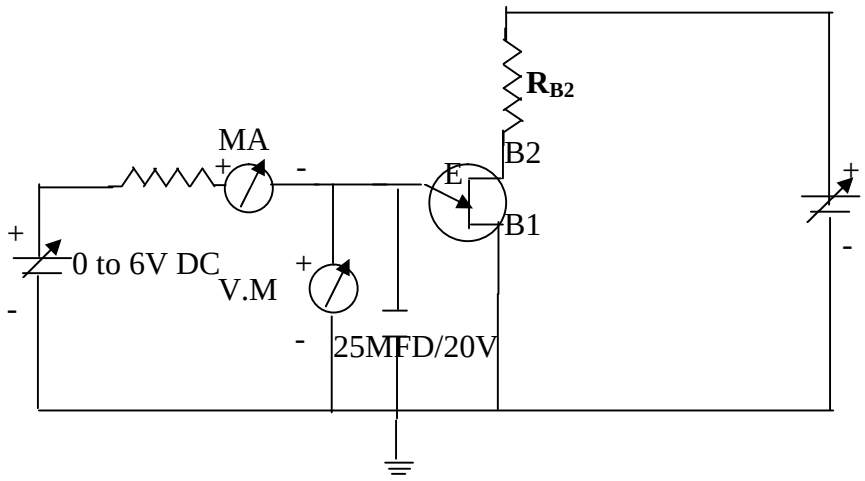


Fig3: Circuit for measurement of I_P, V_P and V_V of UJT

The emitter voltage V_E is increased and the emitter current is noted for a constant V_{BB}. The experiment is repeated for different values of V_{BB}. From graph V_p can be noted. For different values of V_{BB}, we will be able to notice that as V_{BB} increases V_p also increases. The observations are recorded. The experiment is repeated for different values of supply voltage in the range 6-12V.

Observations:

$\mathbf{V_{BB}}$ = 6V

V_{EE}	I_E (mA)

V_{BB} = 10V

V_{EE}	I_E (mA)

Precautions:

1. Proper identification of the terminals of UJT is to be done before making connections to those terminals.
2. Check whether the resistance between B_1 and B_2 lies in the range 5k Ohm and 10k Ohm. It is too low or too high; the device may be defective.
3. All maximum voltage of V_E and V_{BB} the current in the device should not exceed values specified in the data manual.

Result:

The calculated value of η=

η value given in manufacture tools =

Experiment No. 3

UJT RELAXATION OSCILLATOR

Aim: To construct a relaxation oscillator using a unijunctiion transistor (UJT 2N2646), which generate saw tooth waves of different frequencies at emitter and positive pulse at one base and negative pulse at another base.

Apparatus:

1. DC power supply	+6 to 10V	1
2. Resistances	470 Ohm, 100 Ohm	1 each
3. Capacitances	0.002μf, 0.022μf, 0.047μf	1 each
4. CRO		1
5.UJT	2N 2646	1

Theory: A unijunction transistor can be used to construct the relaxation oscillator. The frequency can be set by using the required Rt and Ct taking in to consideration the stand–off ratio of the used UJT.

The frequency $f_0=1/[R_tC_t \ln(1/1-\eta)]$ ----------(1)

Or $T=2.303\ R_tC_t \log (1/1-\eta)$.

The basic unijunction oscillator circuit is given in FIG.1

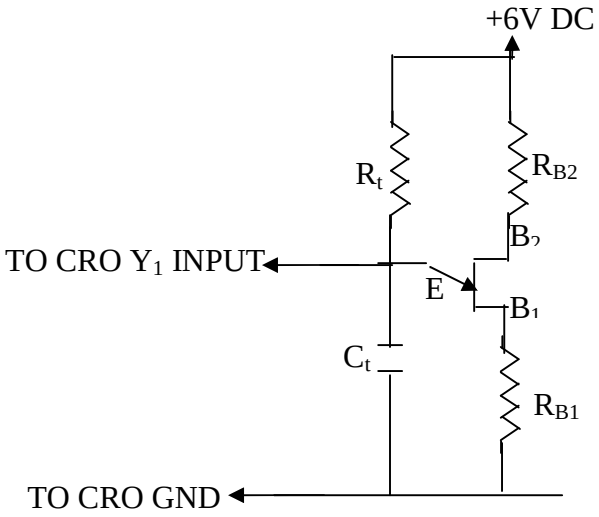


FIG 1

The output waveform observed on CRO is as shown in figure.

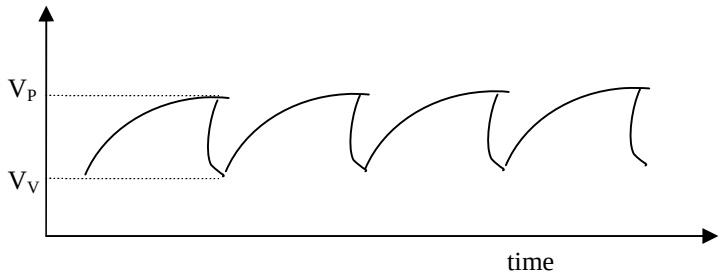


FIG 2

Procedure: The connections are made as shown in the FIG.1 C_t is a variable capacitor whose value can be changed as desired. A DC power supply of +6V DC is applied to the circuit as shown in the fig.1. For different values of C_t the waveforms are observed in CRO and the values of V_v and V_p are noted. The values are recorded in a tabular form. The frequencies are computed using equation given below. The values of observed frequencies and calculated frequencies are compared. They can be observed to be almost the same with in the limits of experimental error. For 2N2646 eta value is 0.689

The value of $1/1-\eta = (V_{BB} - V_v)/(V_{BB} - V_p)$ may also be used in the formula for frequency determination.

Tabular form

S.No	R_t	C_t	Observed frequency (1/T)	Calculated frequency $F=1/2.303R_tC_t\log(1/1-\eta)$

Precautions: 1. The connections are checked before giving power.
2. The soldering should be made properly
3. The A.C or D.C coupling slide switch of channel on which the waveform is observed, is to be kept at D.C. setting.

4. Measure the d.c voltage accurately using a DMM.
5. Display only one or two cycles of the waveform.
6. Always use very fine waveform for taking the observations.

Result: The calculated frequencies and observed frequencies are given in Table. Out of --- observations in --- observations the calculated values are larger than observed values. --- calculated values are less than observed values. --- observations are agreeing with in 5% of the calculated values.

Experiment No. 4

RC COUPLED AMPLIFIER

Aim: -To construct a RC coupled amp (Transistor version) and study its frequency response with and with out feedback.

Apparatus: - Transistor BC 107, resistances33kΩ, 2.2kΩ, 1kΩ, 10kΩ, Capacitances2.2μf, 1μf, 50μf/65V, Signal generator, DC Power supply

Theory: -

An amplifier is a device by which one parameter like voltage, current or power of the given signal at input circuit can be increased and obtained at the output terminals by proper selection of the operating point of the transistor. There are several types of classifications of amplifiers basing on

1.Purpose: (Voltage amplifier, current amplifier. Power amplifier)
2. Coupling circuit: RC coupled , Inductance coupled, Transformer coupled
3.Operating point (Class A, Class B, Class C, Class AB)

In order to increase the amplification we can have multistage amplifiers. Here we take a single stage amplifier and study its performance. If some part of the output (current or voltage) is taken and fed to the transistor along with the input it is called feedback amplifier.

In case of RC coupled amplifier the voltage amplification ($A_v = V_{out}/V_{in}$) is plotted against frequency of the input we get a curve as shown in FIG 1

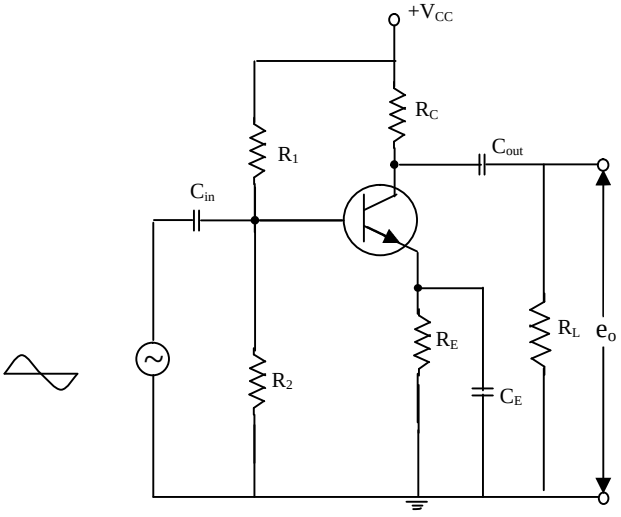
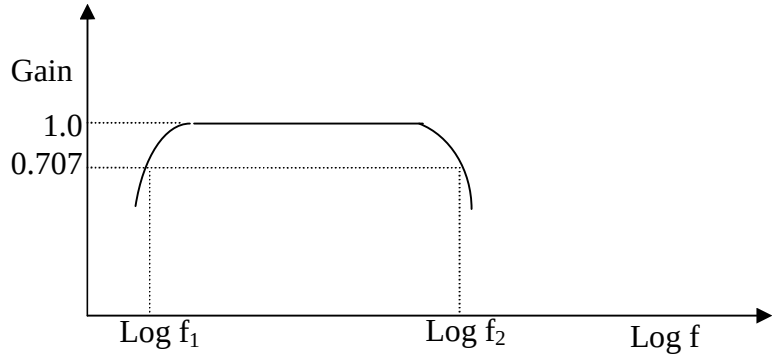


Fig 1 A single stage R-C coupled amplifier.

In a range of frequencies A_v is found to be constant and will not vary with the frequency. At low frequencies the amplification increases with increase of frequency and at high frequencies it falls with the increase of frequency. The circuit diagram is given below (FIG 2).



Normalized gain – frequency response curve

FIG 2

The behavior can be understood as follows.

Low frequency region: The reactance of coupling capacitor is quite high($1/\omega C$) at low frequencies and thus the output decreases with the decrease of frequency in low frequency region. Further, C_E cannot effectively shunt to emitter resistance R_E. These are the two reasons that cause the fall in amplification in the low frequency region.

High frequency region: At high frequencies, the reactance of C_c is very small and behaves as short circuit. If there is a second stage this increases the loading effect and thus decreases the gain. Further, capacitive reactance of base emitter junction at high frequencies becomes low, which increases the base current. This reduces the amplification factor. By these reasons, gain falls at the high frequency region.

Mid frequency region: The voltage gain in this region remains constant. The effect of coupling capacitance is such that it leads to increase in the gain by offering less reactance with increase of frequency, but at the same time this lower reactance loads the first stage and tends to decrease the gain.Thus these two effects mutually annul each other and maintain uniform gain over the mid frequency region.

The frequencies where the gain is 70.7% of the maximum gain are called cutoff frequencies. There are two such frequencies f_1 and f_2 one on the lower frequency side and the other on the higher frequency side. Bandwidth $=(f_2 - f_1)$. On decibel scale the power reduction is of three decibels.

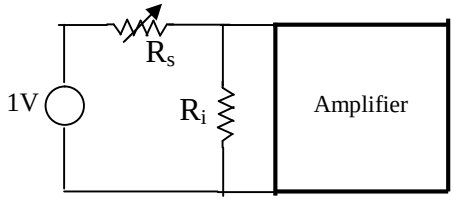
Procedure:

Plotting frequency response curve :

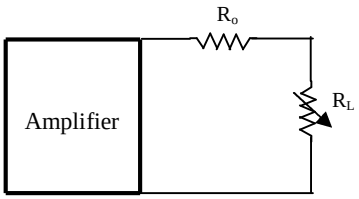
Circuit should be connected as shown in the figure. 30mV (peak to peak) is applied to the base emitter using signal generator. Now measure the output voltage by varying the frequency from 50Hz to 1MHz. Firstly the output voltage increases and reaches a constant value. It remains constant up to a certain frequency and then it decreases. Measure the input and out put voltages in the range 50 Hz to 2Mhz and calculate the gain in dB. After completion of taking readings draw graph taking log f on x axis and gain on Y axis. It is called frequency response curve. Note the 3 db points and determine f_1 and f_2.

Measuring the input and output resistances:

Connect the circuit as shown in fig. Measure the generator voltage and voltage across R_s. As R_s is varied from zero in steps of 100 ohms the voltage acroos it increases. Note the value of R_s at which V_i is equal to$V_s/2$. At this value $R_i=R_s$



For output resistance put decade box at output and vary that until it comes to $V_o/2$. It is the output resistance R_o.



Repeat the experiment after removing the condenser C_E for studying frequency response of RC coupled amplifier with feedback

Observations:

FREQUENCY	OUTPUT VOLTAGE(V_o) volts	Gain V_o/V_i	Gain dB $20 \log (V_o/V_i)$

Precautions:

.

1.Loose connections are to be avoided.
2.Readings must be take carefully on C.R.O.
3. At each observations the input voltage magnitude maintain at 30mv peak to peak.

Result:

Band Width obtained from the graph = kHz.
Input resistance R_i = k Ohms.
Output resistance R_o = k Ohms.

Experiment No. 5

DC REGULATED POWER SUPPLY

Aim: To construct a regulated power supply using a transistor and study its performance.

Apparatus: Transistor BC107, ECN 055 power transistor, resistance box, 0-500 milliammeter, Dimmerstat

Theory:

A DC power supply, constructed using a full wave rectifier with filter circuit still suffers with some disadvantages like

1. Poor regulation: If the DC output voltage varies with load current it is said to have poor regulation.
2. The DC output voltage varies with AC line voltage.
3. The DC output varies with temperature.
4. The ripple voltage, though reduced by filter, the dc voltage is not completely free from it.

To overcome these difficulties a regulator is introduced between the unregulated supply and the load. The following are some of the types of regulators

1.Shunt regulators
2.Series regulators
3.Switching regulators.

Here we discuss the construction of a regulated power supply using series regulator. The series transistor T_1 (called pass transistor) is operated as an emitter follower and appears in series with the load resistance. Hence this regulator is called series regulator. In series regulator the regulation is achieved by comparing a sample of output voltages with a reference voltage. The reference voltage is taken across a zenor diode (V_z). The comparison is carried out by dc amplifier, which produces a signal proportional to the difference between sample voltage and Vz (zener voltage)

A part of the output voltage V_o is sampled by means of the potential divider R_1 and R_2 (see FIG 1). The voltage across R_2 $=\beta V_o$ where $\beta = (R_2/R_1 + R_2)$. This fraction of output is fed to the base of the transistor T_2. The emitter of T_2 is connected to Zener diode and therefore is at a fixed voltage, V_z, which is the reference voltage.

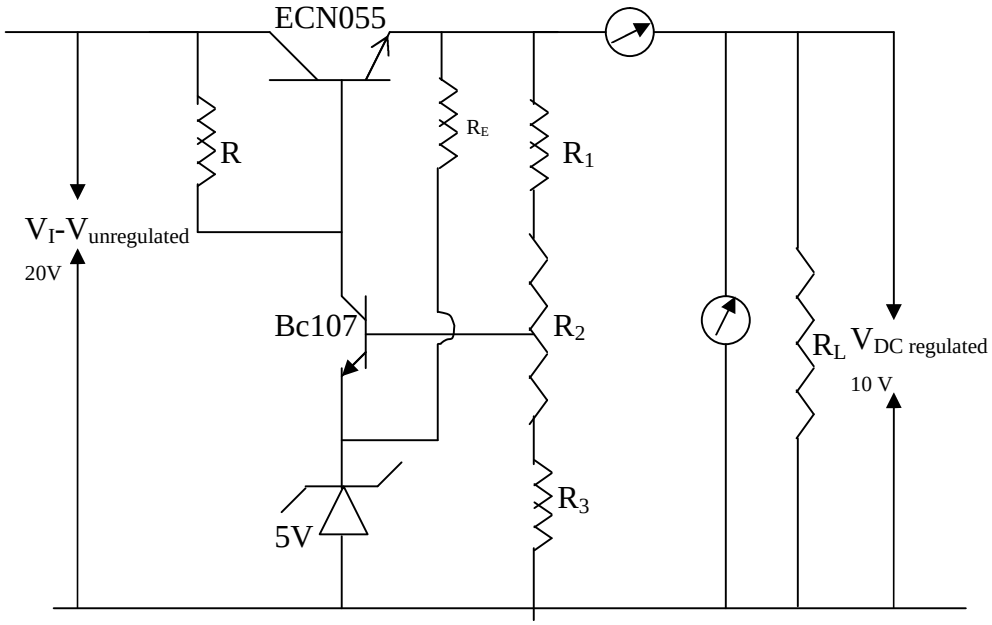


FIG 1

Due to any reason let the output voltage V_0 go up. Then βV_0 also goes up. Thus the base-emitter voltage of T_2 goes up. This will increase the base current of T_2 and consequently collector current of T_2 also increases. This increases the voltage drop across the collector resistance R of T_2 due to its increased collector current. This decreases the bias voltage of T_1. Due to emitter follower function the emitter voltage of T_1 decreases. Thus this is a change in opposite to the original change of V_D. Thus the output voltage remains constant.

Regulation with load:

Procedure:

1. Connect the circuit as shown in the figure.
2. Before making connections we have to identify the collector and emitter and base of the power transistor ECNO55.
3. Connect an an unregulated power supply of 20 V DC (see Fig 2) to the regulator section . Keep the ac input to the unregulated supply at 220V AC Adjust the output voltage to 10V DC by varying the potentiometer.
4. By varying R_L measure the output voltage as a function of load current. Change the load resistance such that the load current changes in steps of 10mA.
5. The input and output voltages are measured by using digital multimeter

Regulation with line voltage:

1. Fix the load current at an optimum value say 50mA.
2. By using a Variac (Dimmerstat) change the AC input of unregulated supply in steps of 10V from 210 – 260 V. In each case measure the input and output voltages.
3. A graph is drawn by taking line voltage along X-axis and unregulated input and regulated output voltages along Y-axis.

% of regulation is defined as the percentage change in output voltage when load is removed

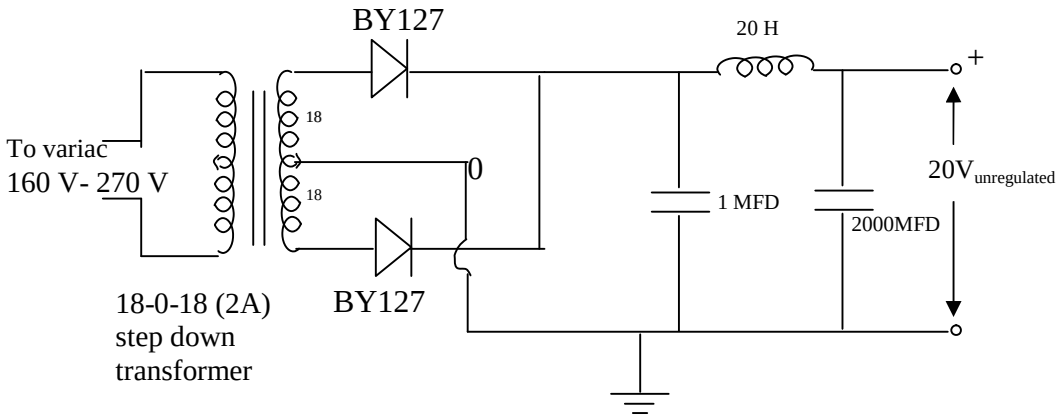


FIG 2: UNREGULATED DC SUPPLY

Observations:

Regulation with load current:

% of regulation= $(E_{0\ noload}-E_{\ 0\ full\ load})/E_{0\ full\ load}$

s.no.	Load current (mA)	Unregualted input voltage E_l	Regulated output voltage	% of regulation unregulated input voltage	% of regulation regulated output voltage

Unregulated input voltage without load = Volts

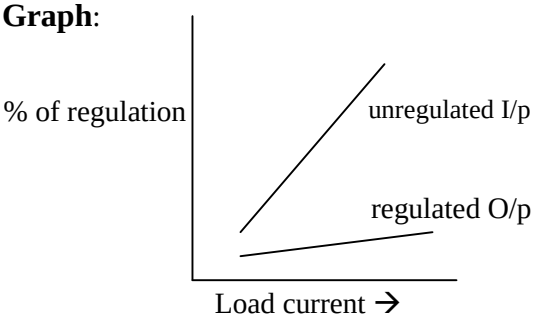
Regulation with line voltage at load current 300mA

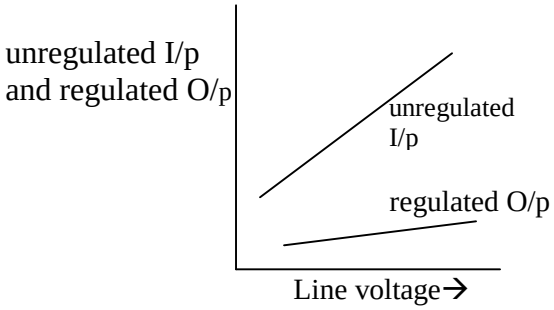
Sl.no.	Line voltage (V)	Unregulated input voltage (V)	Regulated output voltage(V)

The unregulated output voltage without load = Volts

For the ECN055 body of the transistor acts as collector . When fixed to metal chasis its body must be isolated from ground through graphite spacer . A heat sink will enable to draw large current (500mA).

Graph:





Precautions:

1. Measure the voltages with the same meter and in the same setting.
2. Do not use a decade resistance box as load box as the resistances are not meant for high current use. The resistance may be burned and thereby will spoil the box.
3. Connect the unregulated power supply which has the required current delivering capacity to the regulated supply section.

Result:

A transistorized version of dc power supply voltage 10 V is constructed and its regulation with load current up to 450 mA line voltage is studied.

Note to teachers :

Students may be asked to study regulation at different output voltages.

Students may be asked to study the variation of output voltage with change in reference voltage(by changing Zener diode.).

Students may be asked to study the performance of the circuit with and without heat sink to series pass transistor.

Experiment No. 6

ASTABLE MULTIVIBRATOR

Aim: - To construct an astable multivibrator and to generate square waves of different frequencies and to compare the calculated frequencies with the observed ones.

Apparatus:

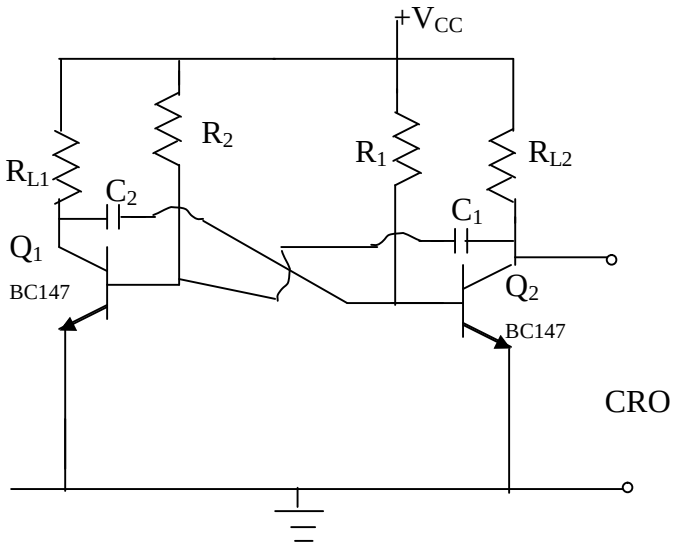
Material	Quantity
Transistor BC 147 or 547	2
Resistors 68kΩ 2.2kΩ	1
Capacitors 0.01μf, 0.022μf, 0.047μf	1
Dc power supply(0 to 30V)	1
Multimeter	1
CRO	1

Theory: A multivibrator is two transistor amplifier circuit with cross coupling. It is used to produce pulse wave form. One of the outputs of a bistable circuit is always high and that of the other is always low. The system remains like that until a steering pulse applied to the bases of the transistor changes the state. After the change of state the transistor whose output was high goes low and remains like that until another pulse changes the state. Thus a bistable multivibrator has two stable states. This results because of the direct cross coupling. If one of the stages is connected to the other capacitively , on receipt of a external triggering pulse a transistor that has high output goes low for some time determined by the time constant of RC network and after that it goes to high state. So for this transistor there is only one stable state and the other is meta stable. Such a circuit is called monostable multivibrator. . It is used as a pulse stretcher. If both the stages are cross coupled capacitively, a transistor which has high at its out put at a given instant goes low depending upon the time constant of the driving transistor and goes low. It cannot stay in that state permanently in that state as in the case of monostable multivibrator because the other time constant forces this transistor to change its state. This process continues indefinitely and we say that it has no stable state or it is an astable multivibrator. An astable multivibrator is some times referred to as free running multivibrator. It is used as square wave generator. Bistable multivibrator remembers in which state it was latched. So, it is also called a flip-flop or latch or 1 bit memory.

Astable multivibrator can be constructed by using different devices

1. Using transistors
2. Using operational amplifier
3. Using 555 timer IC.
4. Using NOR gates (digital astable multivibrator

Circuit diagram:



Working:

When the supply voltage V_{CC} is given, both the transistors draw collector current starts and the capacitors C_1 and C_2 start charging up. We know that no two transistors are exactly alike. And hence one transistor conducts more rapidly than the other. The increasing output of Q_1 is connected through a condenser C_1 to the base of Q_2 . This establishes reverse bias for the other and thereby collector current of Q_2 decreases. Then the raising output of Q_2 goes to the base of Q_1 and it becomes more forward biased and hence collector current of it increases. Thus depending upon the time constants involved in a very short time one transistor goes to saturation and the other gets cutoff. Let Q_1 be in saturation and Q_2 is cutoff. Then collector of Q1 is at 0 volts, entire supply voltage drops across $R_{L1.}$ Q_2 is driven to negative voltage and Q2 goes to cut-off with no drop across $R_{L2.}$

This process is repeated and Q_1 and Q_2 get on and off alternately. The voltage waveforms at either of the collector are essentially a square wave. It can be shown that the time for Q_1 is

$T_1 = 0.69\ R_2C_2$ and for $Q_{2,}$ $T_2 = 0.69R_1C_1$ then total time of the wave

$T = T_1 + T_2 = 0.69(R_2C_2+R_1C_1)$

If $C1 = C_2$ and $R_1=R_2$ then $T = 1.38RC$, $f = 1/\ 1.38RC = 0.7/RC$

The minimum value is β to ensure oscillations ,

$$\beta_1 = R_2 / R_{L1} \qquad \beta_2 = R_1 / R_{L2}$$

If $R_1 = R_2 = R$ and $R_{L1} = R_{L2} = R$

$$\beta_1 = \beta_2$$

Procedure:

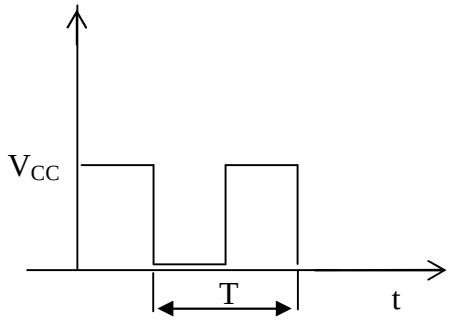
2.2k resistor are used for R_L .68k resistors are used for R. The components are connected as shown in the circuit diagram. Initially the capacitors of value 0.01 μf are used for C1 and C2 . The DC Regulated power supply is adjusted to +6 V D C and then connected to the circuit . A CRO is connected between the grounded , and to one of the collector terminals say, to that of Q_1. If the connections are made properly the circuit starts operating . A square waveforms is observed in the CRO. Make adjustments to obtain stationary pattern following the procedure suggested in practical on CRO operation, we can determine the frequency of the waveform for each value of capacitance. The frequencies can also be calculated for these capacitances using the formula given in equation 1.The theoretical and observed values of the frequencies are compared. Similar procedure is followed for different time constants keeping C fixed and R changed in the range --- to ---.

Observations:

Capacitance value(μf)	Time period T(sec)	Observed frequency f_{ob}=1/T Hz	Calculated frequency Hz

For a given R and R_L values in case the D.C supply for 6V to 12V and record the waveform on any tracing paper.

Graph: Wave form



Precautions: 1. The connections are checked before giving power supply to circuit.
2. The soldering lead must not spread between two terminals.
3. The terminals of the Transistor should be checked.

Result: The calculated frequencies and observed frequencies are in good agreement.

For a given resistance R as the capacitance increases the wave forms developed overshoot / sag .

Experiment No. 7

ZENER DIODE

Aim: -To study the characteristics of a Zener diode and to study Zener diode as voltage regulator.

Apparatus: 0-20 V DC (variable) source, DC voltmeter (0-15V), Ammeter (0-50mA), Zener diode.

Theory:

If we study the characteristics of a semiconductor diode(p-n junction) in reverse bias we notice that there is a reverse saturation current which is of the order of few micro amperes due to the flow of minority charge carriers . As we increase the reverse bias at a certain voltage called break down voltage the current increases suddenly to milli amperes.

This reverse break down may damage the diode permanently. However in certain heavily doped p-n diodes the break down is reversible. The break down voltage is precise and the device may be operated in the breakdown condition. Such diodes are called Zener diodes and

Silicon is usually preferred in the manufacture of zener diodes because of its higher temperature and current capability. Zener diodes are available in the range of 1.8 to 200 volts zener potentials.

Zener breakdown: If the electric field at the junction is sufficiently high, a very strong force will be exerted on the electrons that exist in the covalent bonds and thus the electrons are picked out of the bonds. Then a large number of electrons and holes are generated whose motion caused a large reverse current .This process is known as zener break down . This process can occur due the fields in range of $2x10^7$ volts/meter.

Avalanche break down: In that process the reverse voltage applied makes the minority charge carries acquire sufficient kinetic energy and collide with atoms and ionization process starts. The valence electron then acquires sufficient energy. Those electrons leave the atom and these additional carries aid further additional ionization process. As a result high avalanche current results.

Properties of the Zener diode:

1. A zener diode is always used with reverse bias and in the break down region.
2. Zener break down voltage depends on the amount of doping (also on the semiconductor used).
3. A Zener diode is not burnt when it enters into the break down region, where as an ordinary diode may be burnt when the breakdown is reached.
4. The break down in zener diode is sharp.

It is very inefficient. Power is dissipated in both the resistor and in the zener diode if regulation is to be good, inequality must hold good so that the current through it depends on I_z to a great degree. Thus the efficiency will be quite low. The out put voltage cannot be chosen at will but is dependent on the zener diode.

Study of the characteristics of zener diode:

The connection are made is shown in FIG. 1.

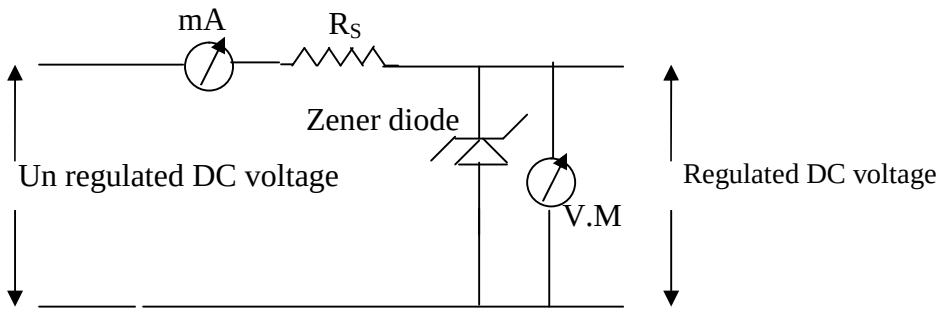


FIG 1

R_S is called the limiting resistance which limits the current in zener diode to its safe maximum value. The milliammeter records the current and the voltmeter (digital multimer preferable), which is parallel to the zener records the voltage across the zener diode. Varying the supply voltage, the zener current, and the corresponding voltages across the zener are noted. Once the voltage across the zener acquires a value, the current (which previously remained almost at zero) suddenly increases. At different values of the current corresponding voltages across the zener (which almost remained constant) are noted. A graph is plotted between the current through the circuit and the voltage across the zener

Zener as voltage regulator:

The circuit for using zener diode as an voltage regulator is shown in FIG.2.

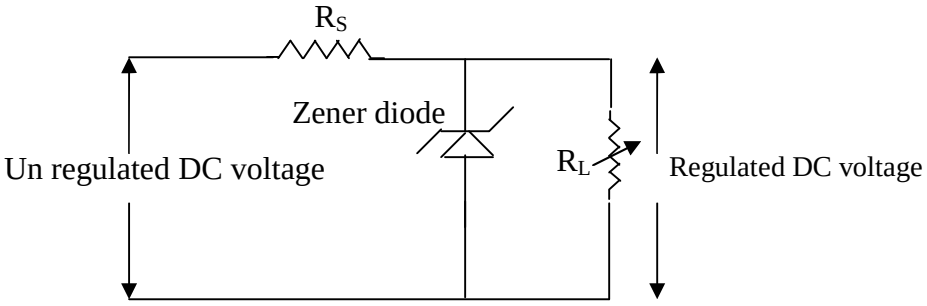


FIG 2

This circuit provides a constant voltage across the load resistance, which is equal to the breakdown voltage of zener used, irrespective of the variations in the supply voltage.

$I_L=(V_z/R_L)$, $Vs=V_R+V_z$

$V_R=V_s-V_z$, $I_R=V_R/R_s=(V_s-V_z)/R_s$

Select R_s such that $I_L<I_R$.

The value of series resistance R_s is to be selected properly to have regulation across R_L. If the series resistance is such that $V_z/R_L=I_L>I_Z$, then the zener circuit gets open and the fluctuation of supply voltage pass on to the load resistance and no regulation takes place.

Procedure: The load resistance is varied and for different load currents the voltages across the zener are noted.

Characteristics:

Zener 1:

V_Z Voltage across Zener (volts)	I Current through Zener (mA)

Zener 2:

V_Z Voltage across Zener (volts)	I Current through Zener (mA)

Zener 3:

V_Z Voltage across Zener (volts)	I Current through Zener (mA)

Tabular form for Zener as Voltage Regulator:

Current through load I_L(mA)	Supply at load V_{LS} (volts)

Precautions: 1. Do not apply the high voltages that cause current through zener diode more than the safe permissible value to the diode.

2. Diode should be connected in reverse bias only.
3. For regulation load should be varied carefully.
4.Do not disconnect the load before switching off the power source.

Result: The characteristics and voltage regulation of zener diode are studied.
The given zener diode is giving regulation at voltage --- and
in the current range-----.

Experiment No. 8

AMPLITUDE MODULATOR

Aim: To construct an amplitude modulator, and to determine the modulation index and percentage of modulation.

Apparatus: Transistor BF494, RF signal generator, Audio generator, CRO, Medium wave coils, driver transformer, capacitors-100pf, 0.047μf, D.C. regulated power supply(0-30 v,1 amp) and 100 k Ohm resistor.

Theory:

1.Introduction:

For successful transmission and reception of intelligence (code, voice, music etc) by the use of radio waves, two processes are essential. They are (i) Modulation (ii) De-Modulation or detection. To modulate means to regulate or adjust. Speech and music etc. are sent thousands of kilometers away by a radio transmitter. Similarly, a scene in front of a television camera is also sent many kilometers away to viewers. In such cases the carrier is the high frequency radio wave. The intelligence i.e. video, sound and other data is impressed on the carrier wave and is carried along with it to the destination.

Modulation is the process of combining the low frequency signal with a very high frequency radio wave called carrier wave (c.w.). The resultant wave is called modulated carrier wave. This job is done at the transmitting station.

During modulation some characteristic of the carrier wave is varied in time with the modulating signal. Accordingly there are three types of sine wave modulations known as amplitude Modulation, Frequency Modulation and Phase Modulation.

The A.M. wave contains three frequency components, a carrier frequency (f_c), one component above the carrier frequency ($f_c + f_s$) and the other component 'below' the carrier frequency ($f_c - f_s$) where 'f_c' and 'f_s' are the carrier and signal frequencies respectively. At the receiver the signal is extracted from the modulated carrier. This process is called A.M. detection or de-modulation.

2. Need for Modulation:

Sometimes, beginners question the necessity of modulation is using a carrier wave to carry the low frequency signal from one place to another. Why not transmit the signals directly and save lot of difficulty? Unfortunately there are the many hurdles in the process of such direct transmission of audio frequency signals. These are

(i) Voice, data and video signals have low frequencies. These waves have relatively short range.

(ii) If everybody transmits these low frequency signals directly, mutual interference will render all of them ineffective.

(iii) Size of antennas required for their efficient radiation would be large, i.e., about 75Km!

Hence, the solution lies in modulation, which enables a low frequency signal to travel very large distances through space with the help of a high frequency carrier wave (f_c). These carrier waves need reasonably sized antennas and care is taken to select the carrier frequencies to avoid interference with other transmitters operating in the same area.

3 Amplitude Modulation:

Definition: When the amplitude of high frequency carrier wave is changed in accordance with the instantaneous value of the amplitude of the signal, it is called amplitude modulation. However the frequency of the modulated wave remains the same i.e at carrier frequency. The following fig (1) shows the principle of amplitude modulation. Fig 1(a) shows the audio electrical signal where as fig 1(b) shows a carrier wave.Fig 1(c) shows the amplitude modulated (AM) wave.

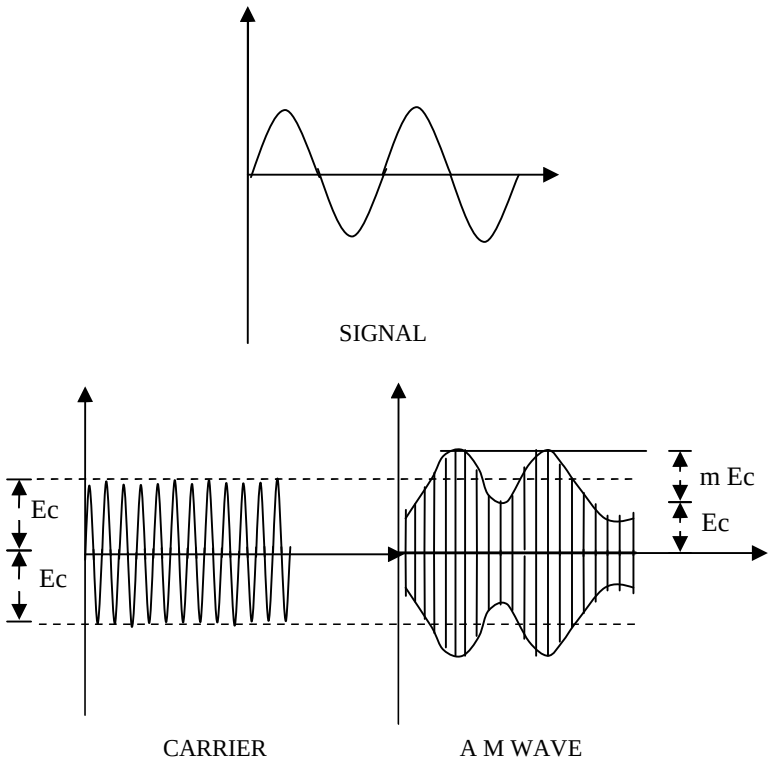


Fig 1.1 Amplitude Modulation

Note that the amplitudes of both positive and negative half cycles of carrier wave are changed in accordance with the signal. Amplitude modulation is done by, an electronic circuit called modulator.

Modulation factor:

An important consideration in A.M. is to describe the depth of modulation, i.e the extent to which the Amplitude of carrier wave is changed by the signal. This is described by a factor called modulation index, which may be defined as under.

Definition of Modulation index / factor:

The ratio of change of carrier wave amplitude due to modulation to the amplitude of un-modulated carrier wave is called the modulation factor m.

4 Mathematical analysis of Wave:

A carrier wave may be represented by $e_c = E_c \cos \omega_c t$, where

e_c = instantaneous voltage of carrier

E_c = amplitude of carrier

$\omega_c = 2\pi f_c$ = angular velocity of carrier of frequency 'f_c'.

The modulating signal can be represented by

$e_s = E_s \cos \omega_s t$

where e_s is the instantaneous value of modulating signal. Es is its amplitude.

$\omega_s = 2\pi f_s$ = angular frequency 'f_s'.

In amplitude modulation the amplitude E_c of the carrier wave is varied in accordance with the instantaneous value of the signal as shown in fig (1.1).

the amplitude of modulated signal can be represented by

$E = E_c + k_a E_m \cos \omega_s t$

Where k_a is called coefficient of modulation

The carrier wave amplitude is varied at signal frequency f_s. Therefore

$$e_c = E_c . (1 + m \cos \omega_s t) \cos \omega_c t.$$

Where $m = k_a E_s / E_c$ is called modulation index or modulation factor

The expression for A.M. wave can be expanded as

$$= E_c . \cos \omega_c t + m . E_c . \cos \omega_s t . \cos \omega_c t.$$

$$= E_c . \cos \omega_c t + m . \frac{E_c}{2} . \{2 \cos \omega_s t . \cos \omega_c t\}$$

$$= E_c . \cos \omega_c t + m . \frac{E_c}{2} \{\cos (\omega_c + \omega_s)t + \cos (\omega_c - \omega_s)t\}$$

$$= E_c . \cos \omega_c t + . \frac{mE_c}{2} . \cos (\omega_c + \omega_s).t + \frac{mE_c}{2} . \cos (\omega_c - \omega_s) t.$$

The following points may be noted from the equation of Amplitude modulated wave.

The A.M. wave is equivalent to the summation of three sinusoidal waves: one having amplitude E_c and frequency 'f_c', the second having amplitude $\frac{mE_c}{2}$ and frequency $(f_c + f_s)$ and the third having amplitude $\frac{mE_c}{2}$ and frequency $(f_c - f_s)$.

The A.M. wave contains three frequencies. They are f_c, $f_c + f_s$ and $(f_c - f_s)$. Thus, the process of amplitude modulation does not change the original carrier frequency but produces two new frequencies $(f_c + f_s)$ and $(f_c - f_s)$, which are called side band frequencies. The sum of carrier frequency and signal frequency i.e.,$(f_c + f_s)$ is called upper side band frequency. The lower side band frequency is $(f_c - f_s)$ i.e., the difference between carrier and signal frequencies. The amplitudes of the side bands are equal and proportional to depth of modulation. It can be shown that the maximum power in each side band occurs when m = 1 and is equal to one fourth of carrier power .

Upper and Lower Sidebands:

In the above discussion, it was assumed that the modulating signal was composed of one frequency component only. However, in a broadcasting station, the modulating signal is the

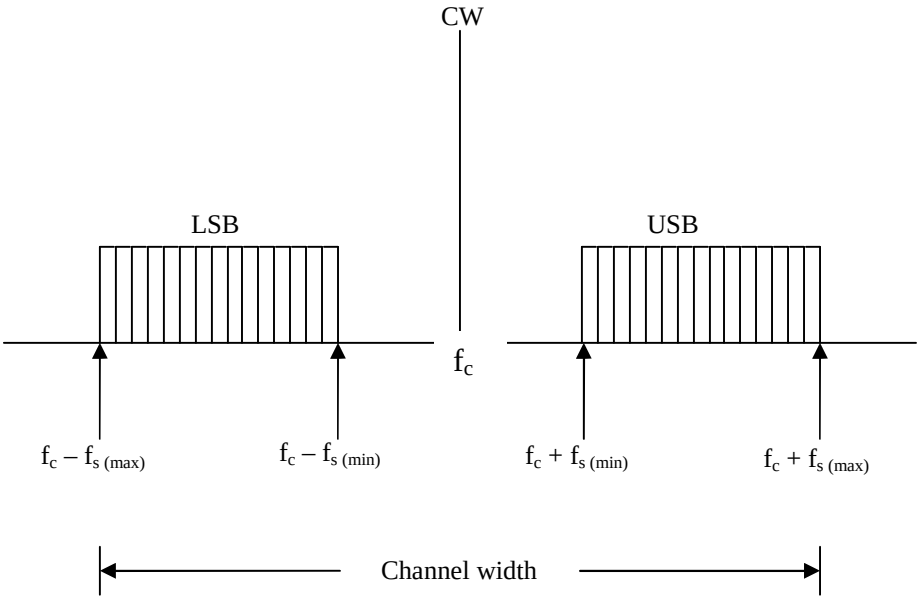


Fig 1.2

human voice (or music), which contains waves with a frequency range of 20-4000 Hz. Each of these waves have its own LSF and USF. When combined together, they give rise to an Upper-side band (USB) and a Lower-side band (LSB) as Shown in fig.

The USB, in fact, contains all sum components of the signal and carrier frequency whereas LSB contains their difference components. The channel width (or bandwidth) is given by the difference between extreme frequencies i.e., between maximum frequency of USB and minimum frequency of LSB. As seen

Channel width = 2 x maximum frequency of modulating signal = 2 x f_s(max).

Example: An audio signal given by 15 sin 2π (2000 t) amplitude-modulates a sinusoidal carrier wave 60 sin 2π (100,000) t.. Assuming k_a=1 determine a) modulation index, (b) percent modulation, (c) frequencies of signal and carrier, (d) frequency spectrum of the modulated wave.

Solution. Here carrier amplitude, A = 60 and modulating signal amplitude B = 15. Therefore

a) Modulation index, $m = \frac{B}{A} = \frac{15}{60} = 0.25$

b) b) Percent modulation, M = m x 100 = 0.25 x 100 = 25%

c) f_s = 2000 Hz --------by inspection of the given equation
f_c = 100,000 Hz --------by inspection of the given equation

d) The three frequencies present in the modulated carrier wave are
(i) 100,000 Hz = 100 kHz,(ii) 120,000 or 120 kHz (iii) 80,000 or 80kHz

Experimentally by measuring the maximum and minimum value of the modulated carrier amplitude one can determine the depth of modulation from the relation

$m = (E_{max} - E_{min}) / (E_{max} + E_{min})$ ----------(1)

From this relation we see that , when $E_{max} = E_{min}$, $m = 0$ or there is no modulation and when $E_{min} = 0$ there is 100 % modulation. In commercial radio broadcasting the depth of modulation is maintained around 40%.

5 Generation of A.M. waves:

Amplitude modulation is produced by combining the carrier and the signal frequencies using a non-linear device. Diodes are non-linear devices but they are not used as they do not offer any gain. Transistors behave as non-linear elements and offer gain as such they are suitable for this applications. Fig 1.3 shows a simple amplitude – modulated amplifier.

The supply V_{CC} in combination with the resistors R_1, R_2, R_C & R_E sets the quiescent point for the transistor. The carrier e_C is the input to the CE amplifier. The circuit amplifies the carrier by a factor A_V where A_V is the voltage gain, so that the amplifier output is $A_V e_C$. The modulating signal e_m is applied in emitter circuit and hence forms a part of the biasing. It produces variations in emitter current at modulating frequency, which in turn produces variations in base emitter resistance and gain A_V. Thus, the amplitude of the carrier varies in accordance with the strength of the signal there by producing Amplitude modulated output across 'R_L'.

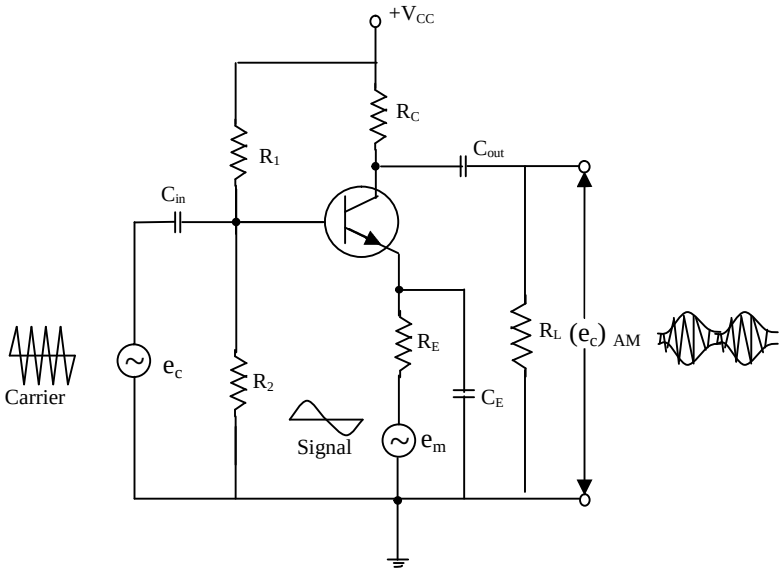


Fig 1.3 An amplitude-modulated amplifier.

Forms of amplitude modulation:

Modulation is a process in which some parameter like amplitude or frequency or phase of a high frequency carrier wave (sinusoidal) is regulated or varied in accordance to the instantaneous value of the low frequency information signal called the Modulating signal.

As there are number of difficulties in transmitting the information signal directly from the place of broadcast to reception center the process of modulation becomes essential. The difficulties are unmanageable size of the antenna power loss and mixing up of different signals etc . 'm' in general lies between 0 and 1. m expressed in percentage is called percentage modulation.

Procedure:-

The modulating signal is applied to base emitter junction using the driver transformer and the carrier signal is applied to the collector base junction using the tank circuit . A DC regulated power supply is used to bias the transistor . Make the connections give the output across the collector and ground Y1 input of CRO. Adjust the time base to nearly the modulating signal frequency. We observe two or three cycles of the modulated signal . By changing the output of function generator amplitude of modulating signal is varied. As the amplitude of modulating signal changes, the depth of modulation also changes. Measure the E max and E min for different depths of modulation . Using these values calculate the modulation index and the percentage of modulation . the amplitude of the modulating signal voltage is measured across the emitter and the ground.

Circuit diagram:

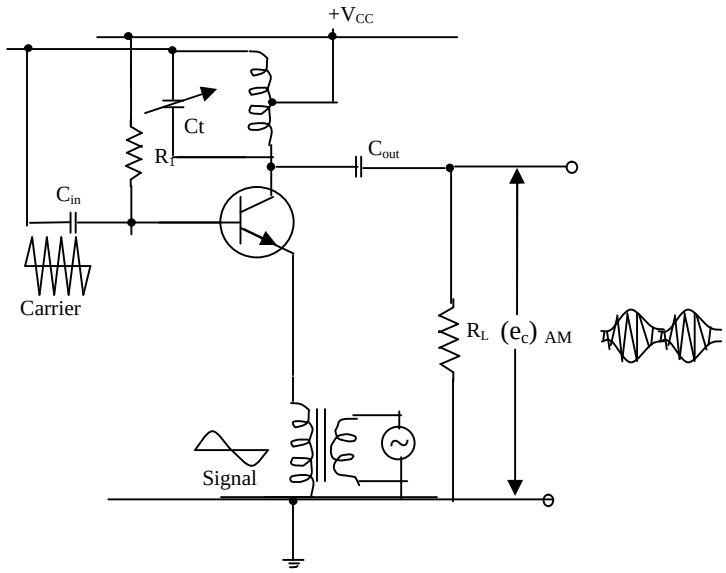
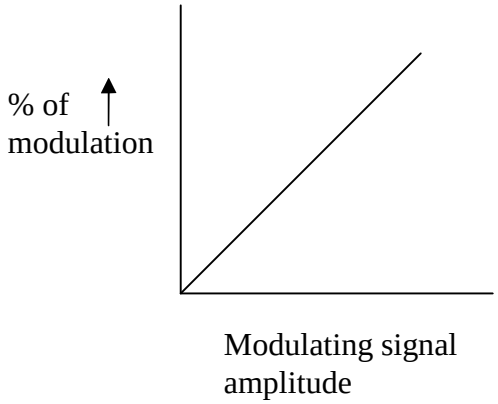


Fig 1.3 An amplitude-modulated oscillator

Observations :

DEPTH OF THE MODULATING SIGNAL AT LOW IMPEDANCE REGION	E max (volts)	E min(volts)	Modulating index (Emax – Emin)/(Emax-Emin)	% of modulation (M.I x 100)

Graph : A graph is drawn by taking amplitude of modulating signal on X-axis and % of modulation on Y-axis. A straight line passing through the origin as shown in fig is obtained



Precautions:

1. Use air gang condenser in tank circuit.
2. Use medium wave oscillator coil with a tap for tank coil.
3. Use at least 100KHz carrier wave and1KHz audio signal for good wave form.
4. Use good regulated power supply to avoid unwanted modulation at power line frequency.
5. Check whether any short between stator and rotor plates of gang condenser before using it in the circuit.
6. Check whether the tank coil and driver transformer, are normal. They should not be open (they should not show very high resistance across their terminals).

Check whether the transistor is in good condition using a transistor checker.

Result: An Amplitude modulation oscillator is constructed and % of modulation is Measured for various amplitudes of modulating signal. The graph obtained is linear indicating that the modulation is linear.

Experiment No. 9

LOGIC GATES

Aim: To study the function of various logic gates by verifying their truth tables.

Apparatus: IC`s with numbers 7432,7400,7402,7404,7408,7486. Bread board, 5V DC power supply, LEDs.

Theory:

Existence of positive voltage at a point may be taken as logic 1. Zero voltage can be represented as logic 0. A glowing bulb, a current flow, a happening of an incident can be represented by logic 1 or TRUE state. The complementary actions can be represented by a 0 or FALSE state. In fact actions that were represented by 1 may also be represented by 0. It all depends on one's choice. The electronic circuits used to perform Boolean operations are called gates. The gate is a circuit with one or more input signals but only one output signal. These gates are constructed by using diodes and transistors (known as DTL logic) or using transistors only (known as TTL). Technical standards were evolved in electronics depending on the implementation of integrated circuits using various semiconductor technologies viz DTL,TTL,ECL etc. The most important and popular semiconductor logic is Transistor-Transistor Logic (TTL), in which a +5V DC is taken as logic 1 and zero volts is taken as logic 0. We learn the fundamentals of Boolean operations, corresponding logic circuits and gates and integrated circuits related to these circuits.

2 Boolean Algebra :

The fundamental operations in Boolean algebra are OR, AND and NOT, with symbols + (plus), **.** (dot) and bubble or bar over Boolean variable respectively.

In real life applications, one combines several logic gates and the combined effect determines a system behavior depending on the states of individual logic variables. This is usually expressed in terms of a truth table. In truth table, various inputs are listed and various combinations are worked out to determine the system behavior. As a simple example, see the OR gate truth table given in table(a). Here A and B are the input variables. These two variables can have 2^2=4 combinations of 1s and 0s. As per the Boolean equation y = A + B (A+B to be red as A or B), output is true for 3 input combinations and false for one combination.

The following are the laws of Boolean algebra and complicated laws can be proved using simple Boolean laws. These laws can be verified by writing truth tables for L.H.S and R.H.S expressions.

1. $A + 0 = A$
2. $A + 1 = 1$
3. $A + A = A$
4. $A + \overline{A} = 1$

} Laws of 'OR'

5. $A \cdot 0 = 0$
6. $A \cdot 1 = A$
7. $A \cdot A = A$
8. $A \cdot \overline{A} = 0$

} Laws of 'AND'

a. $\overline{0} = 1$

9. $\overline{1} = 0$
10. of $A = 0$ then $\overline{A} = 1$

} Laws of complementation (NOT Laws)

3 Basic logic gates:

Basically, a logic gate is a circuit with one or more logic input signals (each input is either 0 or 1), but with only one output signal (logically related to inputs). Logic circuits are analyzed with the help of Boolean laws.

The basic logic gates are: OR, AND and NOT

OR Gate:

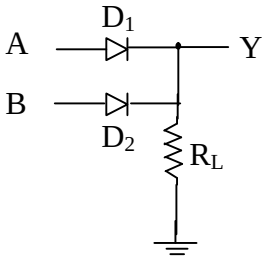
An OR gate has two or more input signals but only one output signal. If one or more input signals are high, the output signal is high.

Boolean expression for two input OR gate is $Y = A + B$

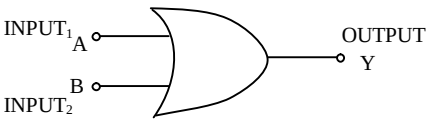
(read as Y equals A OR B).

The circuit to implement the OR function, logic symbol and its truth table (which depicts the output condition to given input is shown in fig (a).

Any one or both of the inputs A, B are high (+5V) makes the corresponding diode to forward bias and the current flows through load resistor R_L to have an output at Y.



Circuit of OR gate

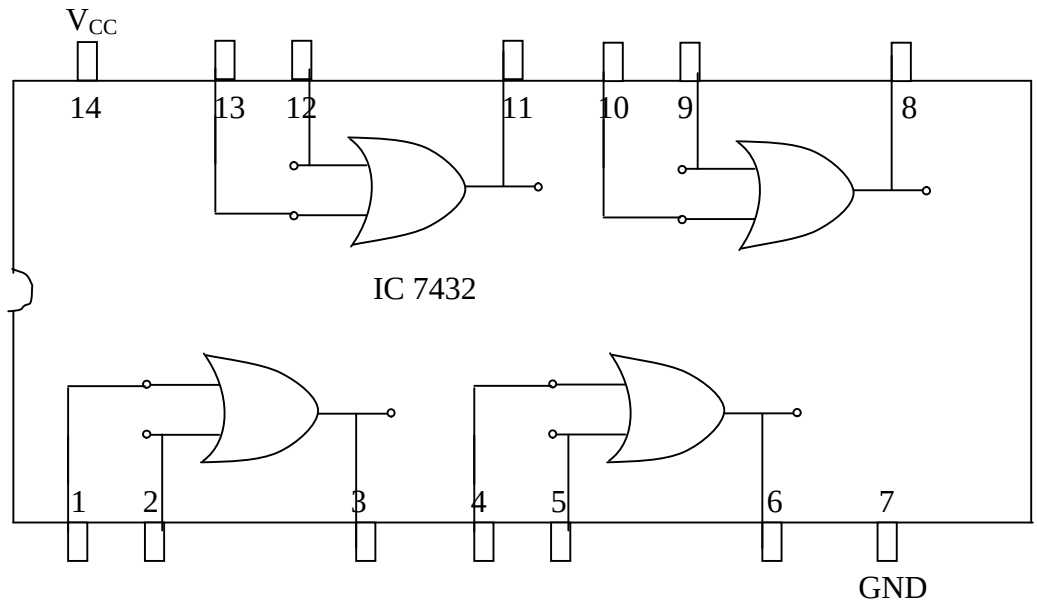


Logic Symbol of OR gate

Fig (a)

TURTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



An OR gate can have any number of inputs 1 to n. For example two input OR-gates can be used to form a 3 input OR gate as shown in fig (b)

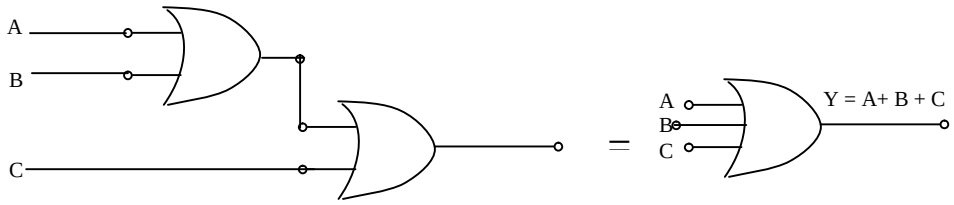
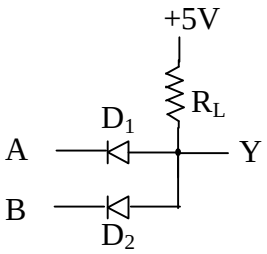


Fig b: Two input OR gates connected to form a 3 input OR gate.

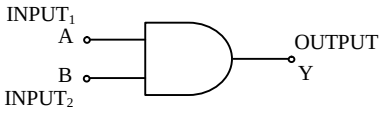
The OR gate circuit of Fig (a) constructed by using diodes and resistors. But the same OR gate can also be constructed by using transistors only (TTL circuit). The logic gates are available in the form of integrated circuits (ICs) to offer advantages in terms of size, cost and power. The IC 7432 is a quad (four), two input OR gate using TTL logic and 74LS32 and 74HS32 are the low power and high speed versions of the same OR gate.

AND gate:

The AND gate has two or more inputs but has only one output. If all the inputs are simultaneously high, the output is high. Boolean expression for two input AND gate is $Y = A \cdot B$ (read as Y equals A AND B). The circuit to implement AND function, corresponding logic diagram and its truth table is shown in Fig (c).



Circuit of AND gate

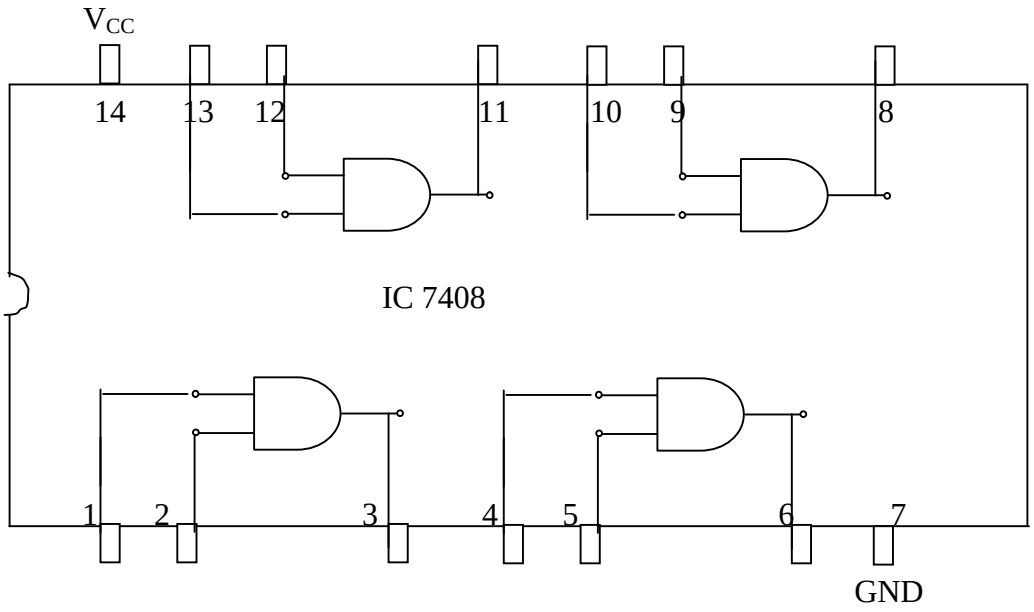


Logic Symbol of AND gate

TURTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Fig(c)



When any one or both of the inputs in above circuit are low, the diode of that input becomes forward biased, so the level of voltage at output point Y is at 0V i.e low state. On the other hand, if both A and B are high, both diodes are now reverse biased and having same voltages at both ends. So 5V appears at Y, i.e high state.

As in the case of OR gate, the two input AND gates can be used to construct three input or n-input AND gate. Construction of 3-input AND gate by using two 2-input AND gates is shown in Fig (d).

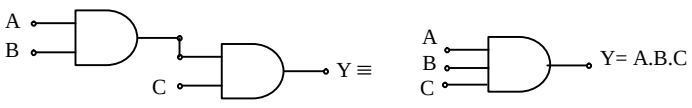


Fig (d)

NOT gate: (Inverter gate):

The inverter is a gate with only one input and one output. The output sate is always the opposite of the input state. It is also called as NOT gate. Boolean expression for this gate is $Y = \overline{A}$ (read as Y equals complement of A or Y equals NOT of A). The circuit, logic symbol and its truth table is shown in Fig (e).

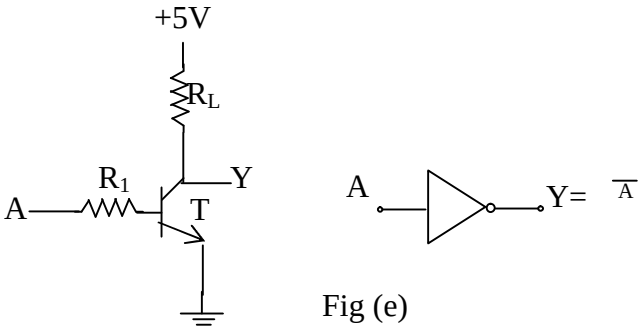
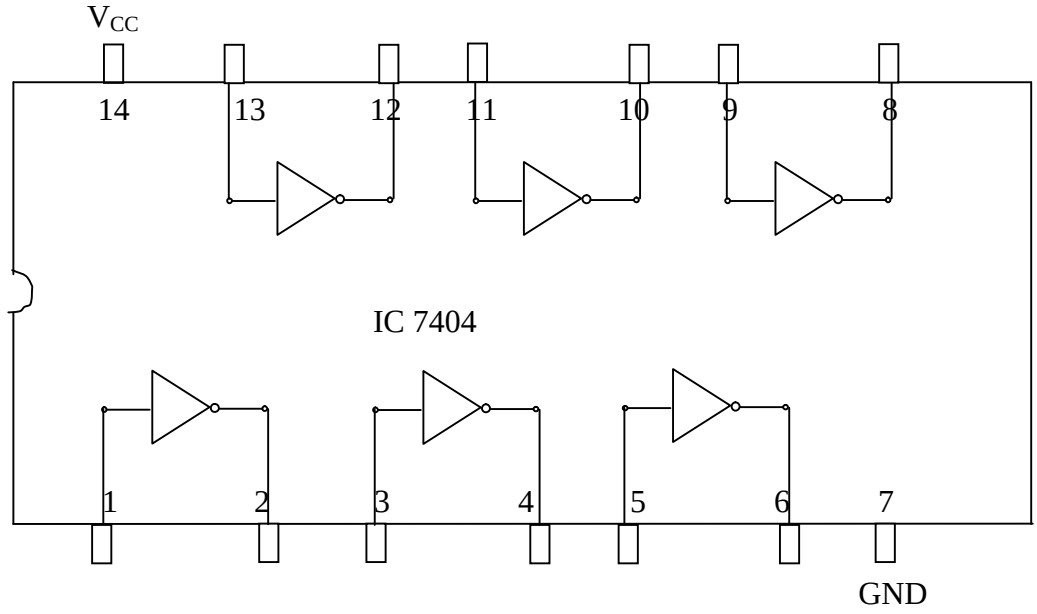


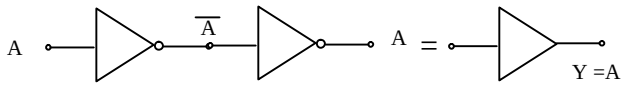
Fig (e)

TRUTH TABLE

Input A	Output Y
0	1
1	0



In the above circuit, the transistor is working either in the conduction or cut-off state. When a high state(+5V) is presented in the input, it makes the transistor to conduct and produce 0V or low state of output. On the other hand, a low state at A produces a high state at y by cut-off the transistor T. Input given to Two NOT gates connected in cascade results in the original Boolean variable as shown in fig (f). This is called a buffer.



TRUTH TABLE

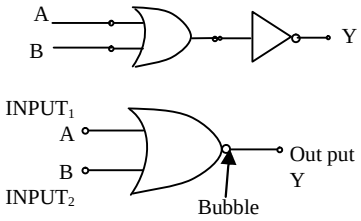
Input A	Output Y
0	0
1	1

Fig (f) Two NOT gates connected to form a buffer, logic symbol of buffer and truth table

Electronically buffers are very useful as they do not alter the nature of original signal but provides boosting of signal amplitude and power to standard levels. This prevents logic failure due to fall in signal strength. Tri-state buffers are also available whose output can be 0, or 1 or tri-state. In the tri-state condition the signal path is disconnected. These tri-state buffers are used in advanced logic circuits like Microprocessors and memories.

NOR gate: The basic logic circuits are used to construct some more gates to perform more Boolean functions. For example, consider the NOR gate which has two or more inputs but only one output. All the inputs must be low to get a high output. Boolean expression for two input NOR gate is $Y = \overline{A + B}$.(read as Y equals not of A OR B).

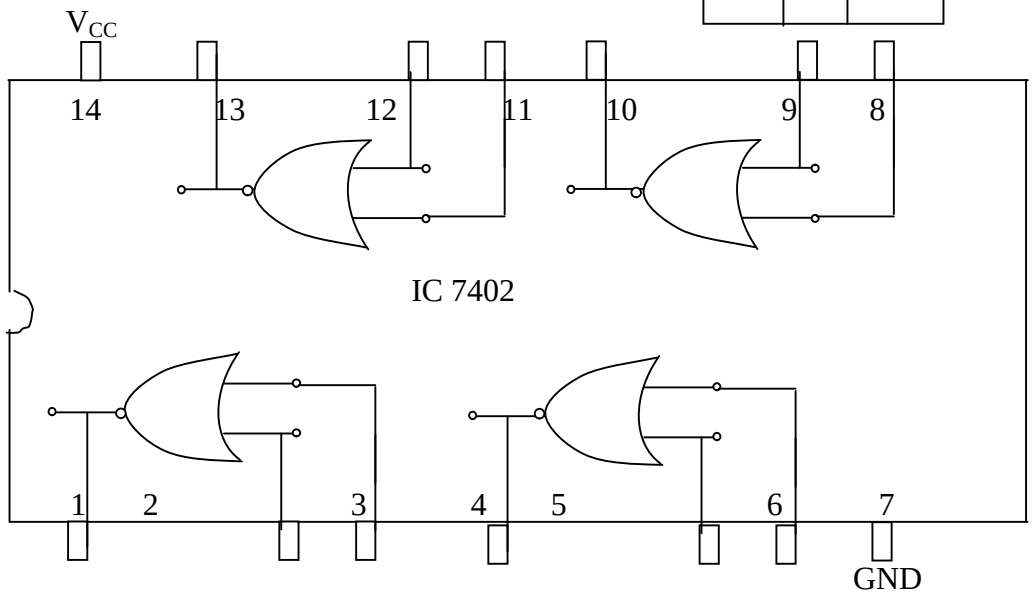
The NOR gate can be constructed by connecting an OR gate with NOT gate as shown in Fig (g)



TRUTH TABLE

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Fig (g)

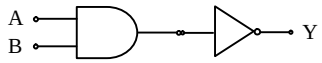


The NOR gate may have more than two inputs. Regardless of how many inputs a NOR gate is still logically equivalent to one OR gate followed by an inverter. For instance, the equation for 3-input NOR gate is $Y= \overline{A+B+C}$. The 7402 is a quad 2-input NOR gate where as 7427 is a triple 3-input NOR gate.

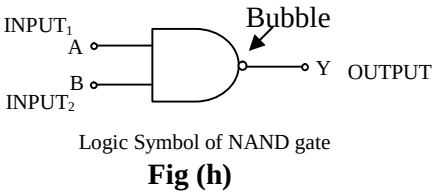
NAND gate:

A NAND gate has two or more inputs but only one output. All the input are the simultaneously high to get a low output. Boolean expression for two – input NAND gate is

$Y = \overline{A.B}$ (read as Y equals Not of A AND B).



The Boolean equations for 3-input and 4-input NAND gates are $Y = \overline{ABC}$ and $Y = \overline{ABCD}$ respectively.

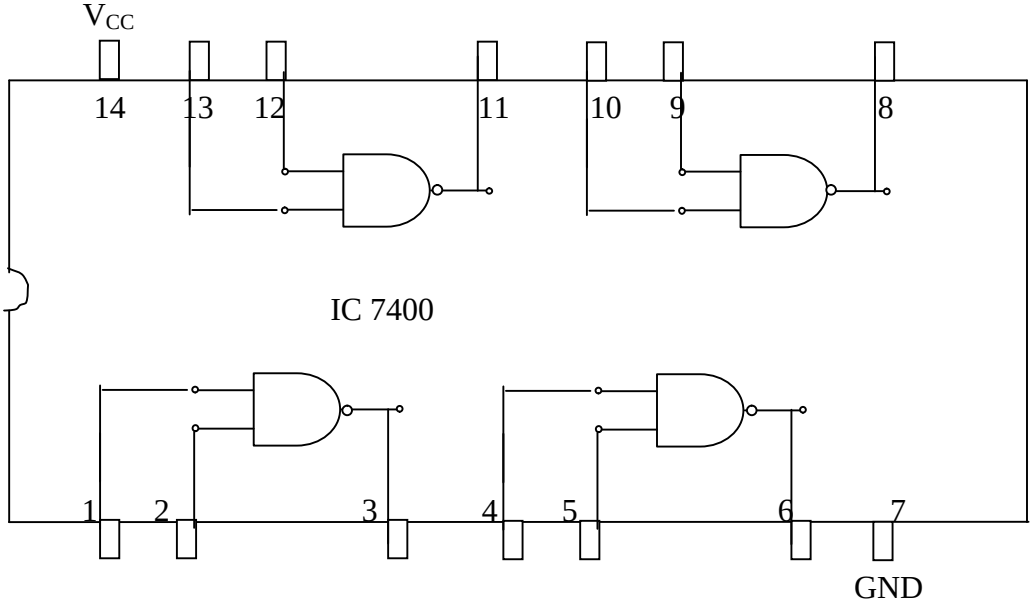


Logic Symbol of NAND gate

Fig (h)

TRUTH TABLE

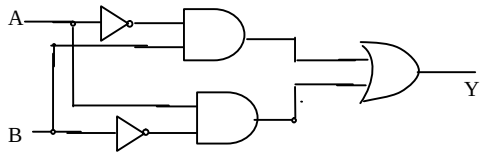
Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

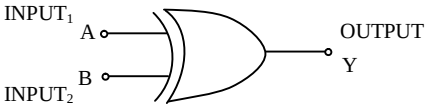


The IC 7400 have four numbers of 2- input NAND gates, whereas 7410 have three numbers of 3-input NAND gates.

EX – OR gate:

An OR gate recognizes words with one or more 1s, whereas the exclusive – OR gate recognizes only words that have an odd number of 1s. Boolean expression for two – input EX-OR gate is $Y = A\overline{B} + \overline{A}B = A \oplus B$ (read as Y equals A EX-OR B). The logic diagram, symbol and its truth table is shown in Fig (i).



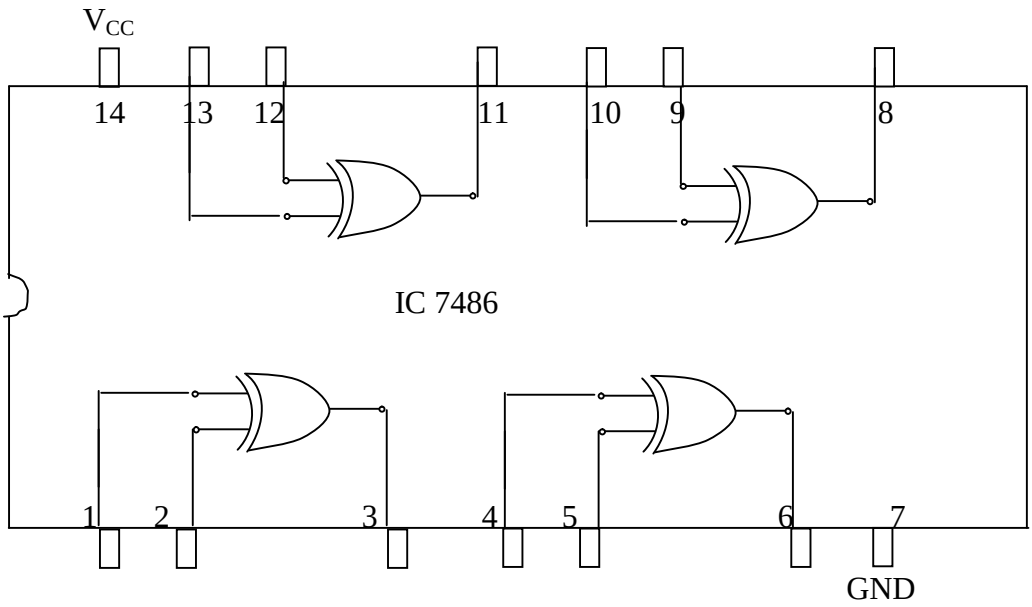


Logic Symbol of EX-OR gate

Fig (i)

TRUTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



When both inputs A & B in the above circuit are high or low both AND gates have low outputs to have the final output zero. But when any one of the input(A or B) is high, the corresponding AND gate output is high. So the final output is one as shown in truth table. IC 7486 is the IC version of EX – OR gate.

Precautions:

1 Use only small length single strand wires of size that fit into the holes of bread board.
2 Don't use thick wires
3 Do not bend the wire ends while inserting in bread board.
4 As there is a possibility of 5V and 0V carrying wires very nearby don't use high current power supplies as the short circuit may damage the bread board.
5 If you want to connect an LED to the output, use always a 1K resistance in series with the diode.
6 Use only exact +5V DC supply while using digital ICs. Don't connect variable voltage supplies to ICs.

Result: The truth tables are verified for the following logic gates and they are observed to be as expected for these gates

Experiment No. 10

COMBINATION OF LOGIC CIRCUITS WITH NAND GATE

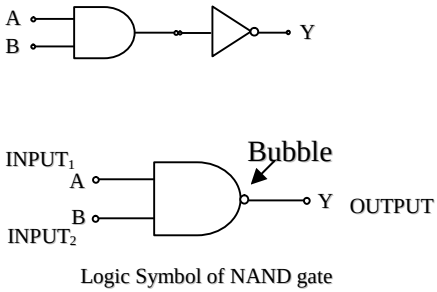
Aim: To construct various logic gates using universal building block NAND gate.

Apparatus: SN 7400 ICs, Bread board, 5VDC fixed power supply, LEDs., 1/8W resistors

Theory:

1 **Forming other logic gates using only NAND gates:**

(i) NOT gate: From the truth table of the NAND gate given in Fig 1,



Logic Symbol of NAND gate

Fig 1

TRUTH TABLE

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

If all the inputs are connected to the same logic NAND gives its complement as output viz if A= B= 0 we have an output of 1 and if A= B= 1, the output is 0. Hence the circuit of Fig (a) acts as NOT gate.

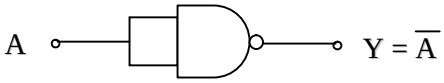


Fig (a)

$y=\overline{A.A}=\overline{A}$

ii) AND gate: The Boolean expression for NAND is $Y=\overline{A.B}$. Complimenting the output of NAND gate results in A.B the logical AND operation. So, in Fig b the first NAND gate output is $\overline{A.B}$ and second NAND gate simply connected as a NOT gate resulting in an AND gate circuit.

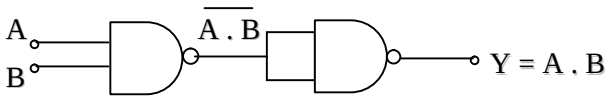


Fig (b)

$y=\overline{\overline{A.B}}=A.B$

(iii)OR gate: The Boolean expression for logical OR operation is A+B . It can be written as $\overline{\overline{A}} + \overline{\overline{B}}$ Using De Morgan theorems it can be written as compliment of ($\overline{A}$. $\overline{B}$). Basically it is an AND gate but the inputs are $\overline{A}$ and $\overline{B}$ instead of A and B . So two not gates to invert inputs and one NAND gate will generate OR operation as shown in fig c.

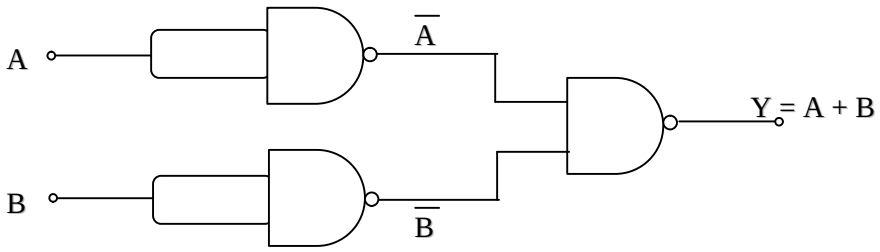


Fig (c)

$Y=\overline{\overline{A}.\overline{B}}=\overline{\overline{A}}+\overline{\overline{B}}=A+B$

(iv) NOR gate:

Addition of another NOT gate to the circuit for OR gate of Fig (c) as shown in Fig (d) gives the operation of a NOR gate.

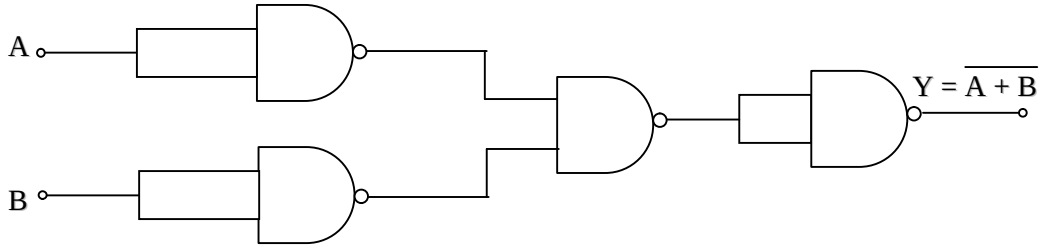


Fig (d)

$Y= \overline{(A+B).(A+B)} =\overline{A+B}$

(v) EX – OR gate: The boolean expression is $Y = A\overline{B} + \overline{A}B$

This equation can be expressed in various forms using De Morgan's laws.

Ex: $\overline{A}B+A\overline{B}$ can be expressed in NAND-NAND form as $\overline{\overline{A.B}.\overline{B.A}}$

. this can be shown using only 4 NAND gates .The logic diagram is given in fig (e).

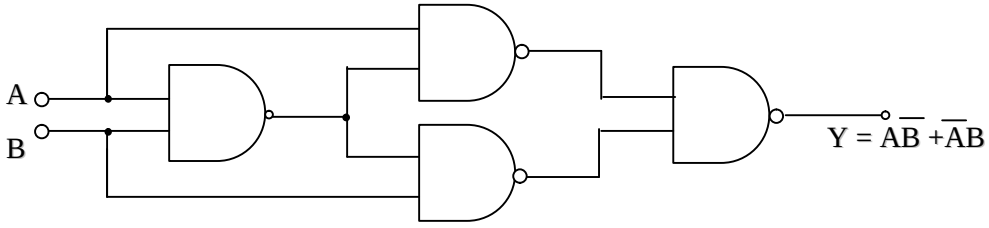


Fig (e)

$\overline{A.\overline{AB}}=A.\overline{A}+\overline{B}=A\overline{B}$

$\overline{B.\overline{AB}}=B.\overline{A}+\overline{B}=B\overline{A}$

$Y=\overline{A.\overline{B}}.\overline{B.\overline{A}} = \overline{A.\overline{B}} + \overline{B.\overline{A}} = A\overline{B}+B\overline{A}$

NOTE: the students may be asked to try other forms

2 Other Logic gates using only NOR gates :

(i) NOT gate : It is easy to verify from the truth table of NOR gate that when all the inputs of NOR are tied together it acts as an inverter.

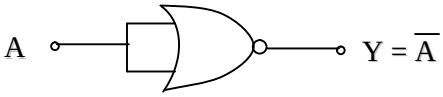


Fig (f)

$Y=\overline{A+A}=\overline{A}$

(ii) OR gate:

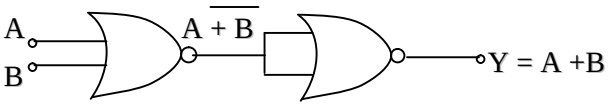


Fig (g)

$Y=\overline{\overline{A+B}+\overline{A+B}}=\overline{A+B}=A+B$

(iii) AND gate:

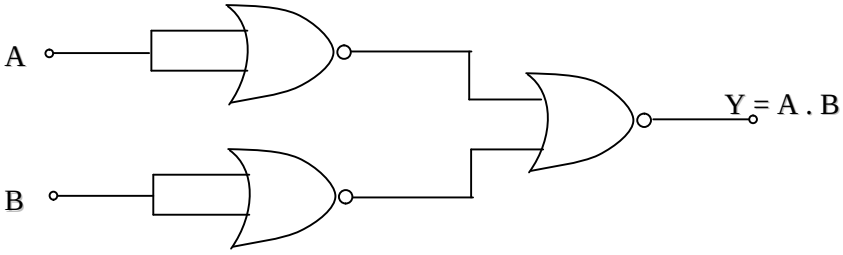


Fig (h)

$Y=\overline{\overline{A+A}+\overline{B+B}}=\overline{\overline{A}+\overline{B}}=\overline{A}.\overline{B}=A.B$

(iii) NAND gate:

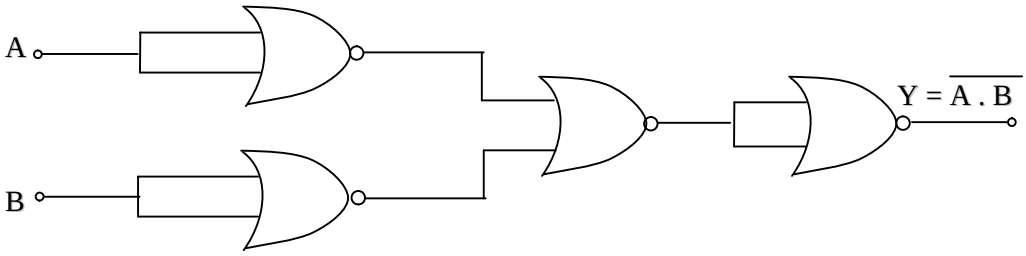


Fig (i)

$Y' = \overline{\overline{A+A}+\overline{B+B}} = \overline{\overline{A}+\overline{B}} = \overline{\overline{A}.\overline{B}} = A.B$

$Y = \overline{A.B+A.B} = \overline{A.B}$

(v) EX - OR gate:

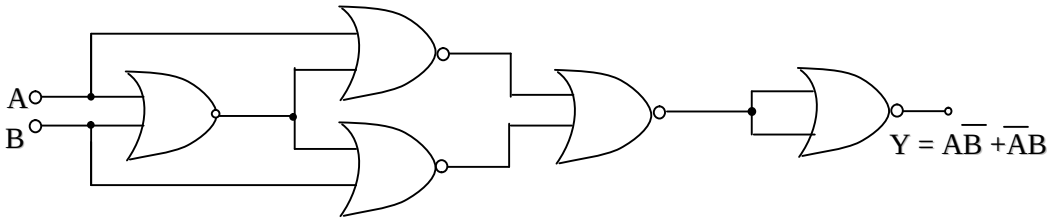


Fig (j)

$Y' = \overline{A+\overline{A+B}}+\overline{B+\overline{A+B}} = A+\overline{A}.\overline{B}+B+\overline{A}.\overline{B}$

$= \overline{A}.\overline{(A.B)}+\overline{B}.\overline{(A+B)} = A\overline{B}+B\overline{A}$

$Y = \overline{Y'.Y'} = \overline{Y'} = A\overline{B}+B\overline{A}$

Of the several technologies available Transistor–Transistor Logic is widely used where logic 1 is represented by +5V DC. And Logic zero by 0V DC. Circuits using other types of logic are provided with TTL logic compatibility to facilitate easy interfacing of logic circuits.

When a logic gate is connected to another logic gate, depending on the logic status it is supposed to supply or take currents. Supplying current is called sourcing and taking the current is called sinking. Capability of a circuit depends on how much current a circuit can sink and source.

This is expressed in terms of how many logic gates can be connected to it (fan-in) and how many circuits can be driven by it (fan-out). For standard TTL fan – out is 10.

Logic circuits are supposed to change their states from 0 to 1 or 1 to 0 instantaneously, but, electronic circuits have inherent delays and because of it, there will be some definite rise time, fall time and propagation delay as a signal passes from input to output. Further there will be signal attenuation and induction effects and noise, which affect signal amplitude. For a standard TTL circuit if a logic 1 signal amplitude falls below 2.4V DC it cannot be recognized as Logic1. Like wise, if logic 0 signal amplitude is greater than 0.4V DC it cannot be identified as logic 0. This

results in failure of logic circuits. Crossing the fan-in and fan-out limits also changes logic voltages. So logic circuits are to be buffered to bring back, the signal levels to TTL levels before they are deteriorated. A signal in its transmission path may develop glitches, slopes and other types of distortion. Schmitt trigger circuit is used to produce rectangular wave shape regardless of the input waveform.

In many circuits the compliment of AND gate output is needed (0 is compliment of 1 and 1 is compliment of 0). It can be obtained by connecting NOT gate at the output of AND gate. The NAND gate diagram is as follows. This gate will give the inverted output or complement output of AND gate.

Precautions:

1. Verify the truth table of individual NAND elements in each IC before using them in the circuit..
2. The connections should be short and correct. Use different colored wires Ex Red for +5v, black for GND, Green for A, Blue for B input, Yellow for output. Select other colors as per your choice and availability.

Result: Truth tables of the constructed logic gates using NAND gate is verified along with ICs. The agreement is good.

Note:

1. Avoid any one of the connections
2. The truth tables should be verified for all the input combinations.

Experiment No. 11

HALF ADDER AND FULL ADDER

Aim: To construct Half adder and Full adder circuits and to observe their operations by verifying their truth tables.

Apparatus: IC's with no. 7432,7408,7404 and 7486, 5VDC powers supply, Bread board.

Theory:

1 Binary addition:

When we perform binary addition and subtraction, the following rules must be followed.

Binary addition	Binary subtraction
$0 + 0 = 0 \rightarrow$ (1)	0 – 0 = 0 barrow 0
$0 + 1 = 1 \rightarrow$ (2)	0 – 1 = 1 barrow 1
$1 + 0 = 1 \rightarrow$ (3)	1 – 0 = 1 barrow 0
$1 + 1 = 10 \rightarrow$ (4)	1 – 1 = 0 barrow 0
$1 + 1 + 1 = 11 \rightarrow$ (5)	

In binary addition the first three operations produce a sum with only one digit, but when both augend and added bits are equal to 1, the binary sum consists of two digits. The higher significant bit of this result is called a carry.

2 Half Adder:

A combinational circuit that performs the addition of two – bits is called a Half – adder. The Half – adder has two binary inputs and two binary outputs.

This is 1 – bit adder. This circuit is called half – adder because it cannot accept a carry – in from previous additions. The inputs to the circuits are the addend and augend bits. The outputs produced by it are sum (s) and carry (c). The half adder can be constructed by using one AND gate and an EX – OR gate. Fig 1(a) shows logic circuit that adds 2 bits namely A and B.
Fig 1(b) shows the truth table of it. The carry output is 0 unless both inputs are 1. The S output represents the least significant bit of the sum.

Boolean equation for sum (s) = $A \oplus B = A\overline{B} + \bar{A}B$.

= A (EX – OR) B

Carry (c) = A AND B = AB

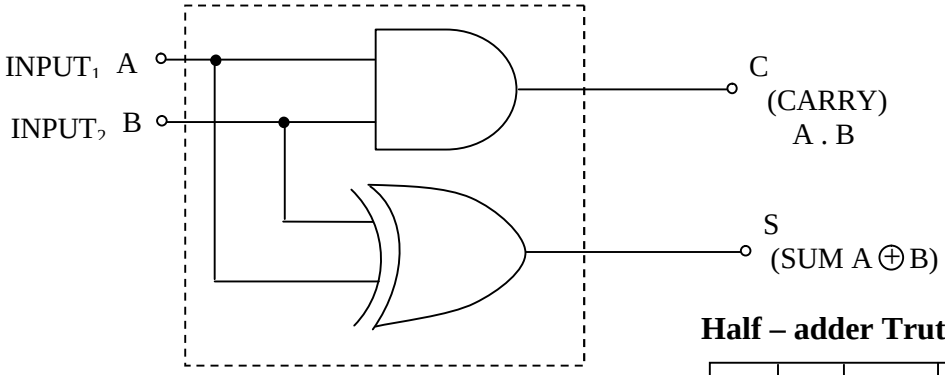


Fig 1(a) Half-Adder Logic circuit

Fig 1 (b) Half – adder Logic symbol

Half – adder Truth table

A	B	Carry C	Sum S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Fig 1 (c)

3. Full adder:

A full adder is combinational circuit that forms the arithmetic sum of three input bits. The two significant bits to be added are denoted as A and B, where as the third input C represents the carry from the previous lower significant position. The full adder can be constructed from two half adders and one OR gate as shown in fig 2(a). and its symbol is shown in fig 2(b).

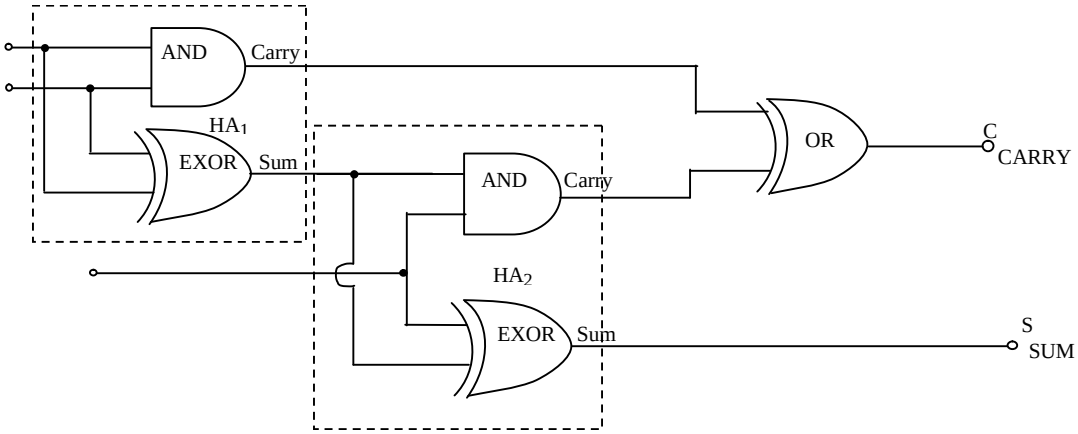


Fig 2(a) : Full – adder Logic diagram

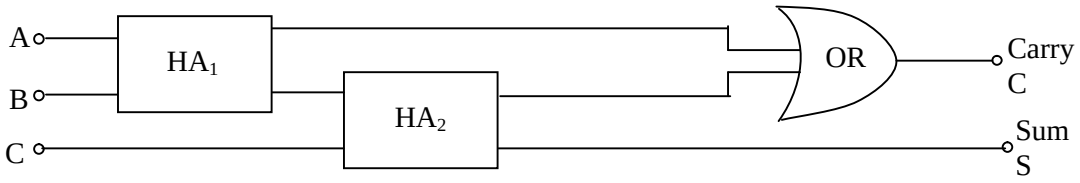


Fig 2 (b): Full – adder Logic Symbol

INPUTS			OUTPUTS	
A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig 2 (c) Full – adder Truth Table

4 Binary four bit parallel Adder:

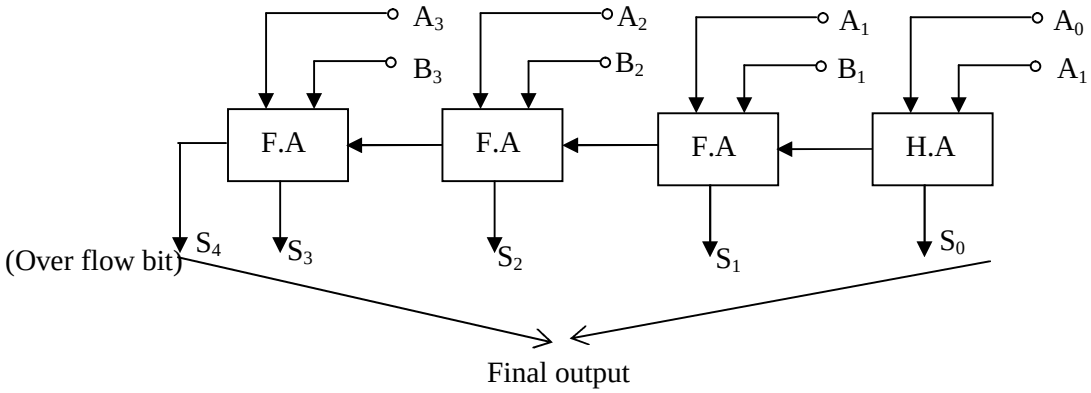


Fig 3

Note: In binary, the count starts from zero rather than from 1. The first bit is called S_0 rather than S_1. Similarly the nyj bit is S_{n-1}.

A parallel adder is an m-bi at a time. This produces the arithmetic sum of two n-bit binary numbers in parallel. This can be constructed by using one half adder and several full adders. The full adders are connected in cascade, with the output carry from one full adder connected to the input carry of the next full adder.

Fig 3 shows the logic diagram for 4-bit parallel adder circuit.

Suppose we want to add 4-bit binary numbers A_3 A_2 A_1 A_0 and B_3 B_2 B_1 B_0 then we get a sum S_4 S_3 S_2 S_1 S_0 where S_4 indicates overflow bit if the sum exceeds four bits. For adding the above two 4-bit numbers, we require three full adders and a half adder connected in parallel. The output (carry) of each adder is connected to next adder to get a parallel adder.

Observations:

For full adder:

Input A	Input B	Input C	Output Carry(C)	Output Sum(S)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

For half adder:

Input A	Input B	Output Carry (C)	Output Sum(S)
0	0		
0	1		
1	0		
1	1		

Precautions:

1. The connections should be correct if any one of the connection is loose then it will give different out put.
2. The truth tables should be verified correctly

Result: The truth tables of assembled half adders and full adders are in agreement with ideal truth tables of half and full adders indicating that the circuit was assembled properly.

Experiment No. 12

Multiplexer and Decoder

Aim: To construct 1. a digital multiplexer and 2.a decoder

Apparatus: IC`s with numbers 7432,7400,7402,7404,7408,7486. Bread board, 5v power supply, LEDs.

Theory:

Decoder:

A decoder is a combinational circuit that converts binary information from 'n' input lines to a maximum of 2^n unique output lines. Decoders are available with several output configurations: active low voltage, high-sink current for direct driving of indicator lamps. Output voltage ratings range from +5V to over +100V. The decoder is used in conjunction with some code converters such as a BCD – to – 7 segment decoder, BCD – to – Decimal decoder. The decoder presented here is called n – to 2^n line decoders decoder. Its purpose is to generate the 2^n min terms of n input variables. These decoders form a combinational circuit with n input variables and 2^n output variables. For each binary input combination of 1s and 0s, there is one and only one output line that assumes the value of 1. Figure (a) shows a 2 by 4 decoder. It has four AND gates and two inverters.

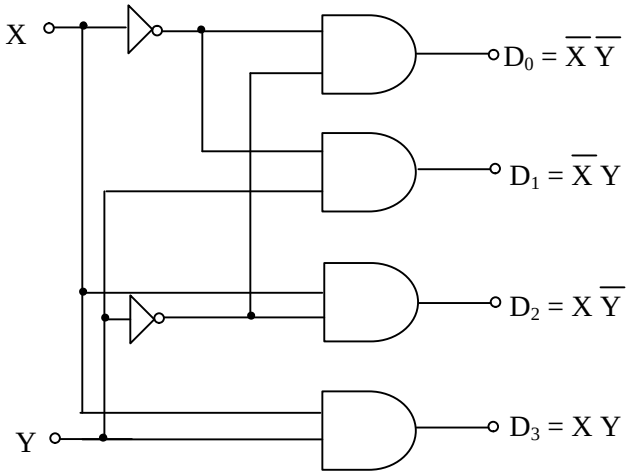


FIG (a) 2 – bit decoder

X	Y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig (b) 2- bit decoder Truth table

Some times an enable input may be included with a decoder to control the circuit operation. In this, all outputs will be equal to 0, if the enable input is zero. When the enable input is 1, the circuit operates as a conventional decoder. Block diagram of 3 to 8 decoder with enable signal is shown in Fig c.

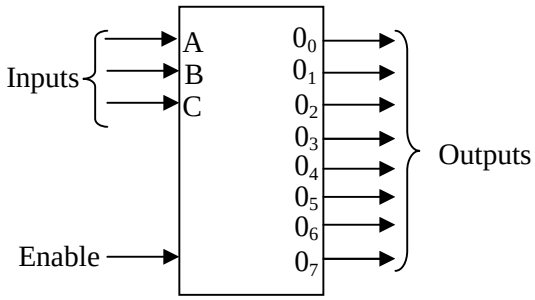


Fig c Block diagram of 3 to 8 bit decoder

Demultiplexer:

A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of a specific output line is controlled by the bit values of n selection lines. Figure (d) shows the block diagram of decoder and demultiplixer. The decoder with an enable input can function as a demultiplexer.

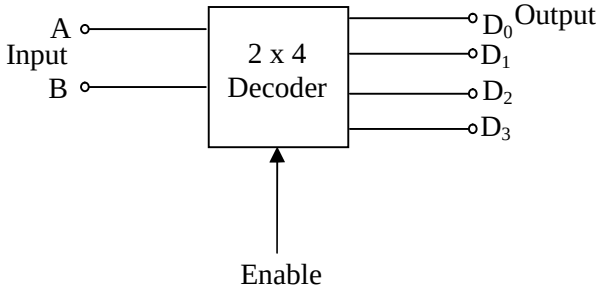


Fig (d)

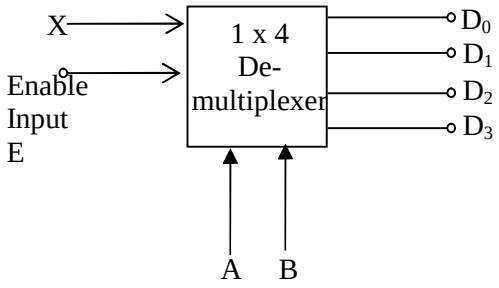


Fig (e)

The decoder of Fig (d) can function as a demultiplexer if the enable line is taken as a data input line and lines A and B are taken as the selection lines as shown in Fig (e). Out of 4 output lines, one gets link with input E depends upon the binary value of two selection lines A and B (i.e), if AB = 01, D_1 gets connected with the input E, so that input is available at D_1 output. While all other outputs are maintained at 1.

Encoder:

An encoder is a digital circuit, that produces a reverse operation from that of a decoder. An encoder has 2^n input lines and n output lines. The output lines generate the binary code for the 2^n input variables. One of the encoders is shown in fig (f). It has eight inputs, one for each of the eight digits and three outputs that generate the corresponding binary outputs that generate the corresponding binary number.

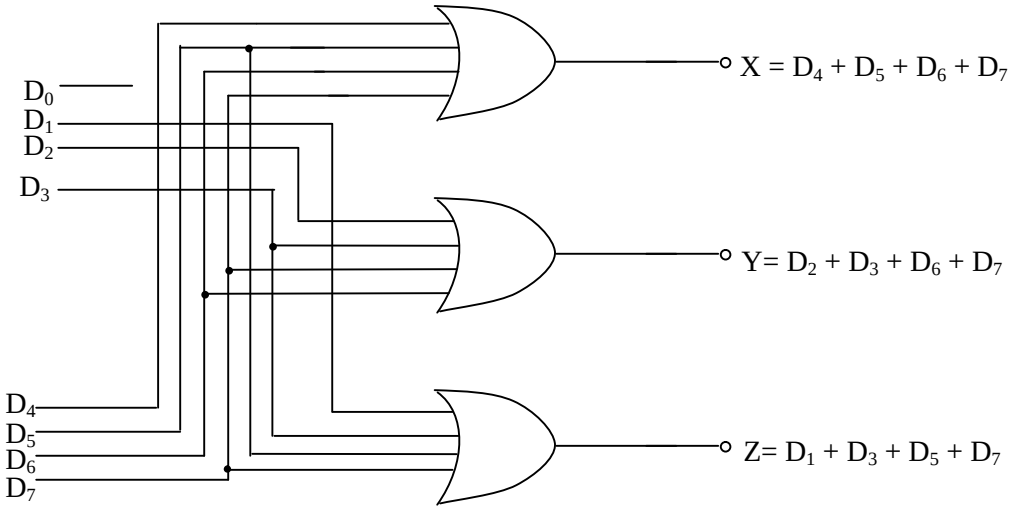


Fig. (f)

Fig (f) shows the octal to binary encoder. It is constructed with OR gates. It, has 8 input lines and could have 2^8 = 256 possible input combinations. Only eight of these combinations have meaning and others are don't care conditions. The output z is 1, if the input digits are odd. Output Y is 1 for octal digits 2, 3, 6 and 7. Output X is 1 for digits 4, 5, 6 or 7. It is 1 at any time. Do is not connected to any OR gate. It arises that only the highest priority input line is encoded.

INPUTS								OUTPUTS		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Truth table (g)

Multiplexers / Data selector:

It is a combinational circuit which selects binary information from one of many input lines and directs it to single outputs line. The selection of a particular input line is controlled by a set of selection lines. For 'n' bits, there are 2^n input lines and n selection lines whose bit combinations determine which inputs is selected. This means "many into one". It is used when a complex logic circuit is to be shaved by a number of input signals. Fig 8 shows the logic diagram, block diagram and function table of a 4 to 1 line multiplexer.

A line to 1 line multiplexer has 4 inputs I_0 to I_3 and one output line. Each of the four input lines is applied to one input of a three input AND gate. The remaining two inputs of it is supplied by selection lines S_1 and S_0.

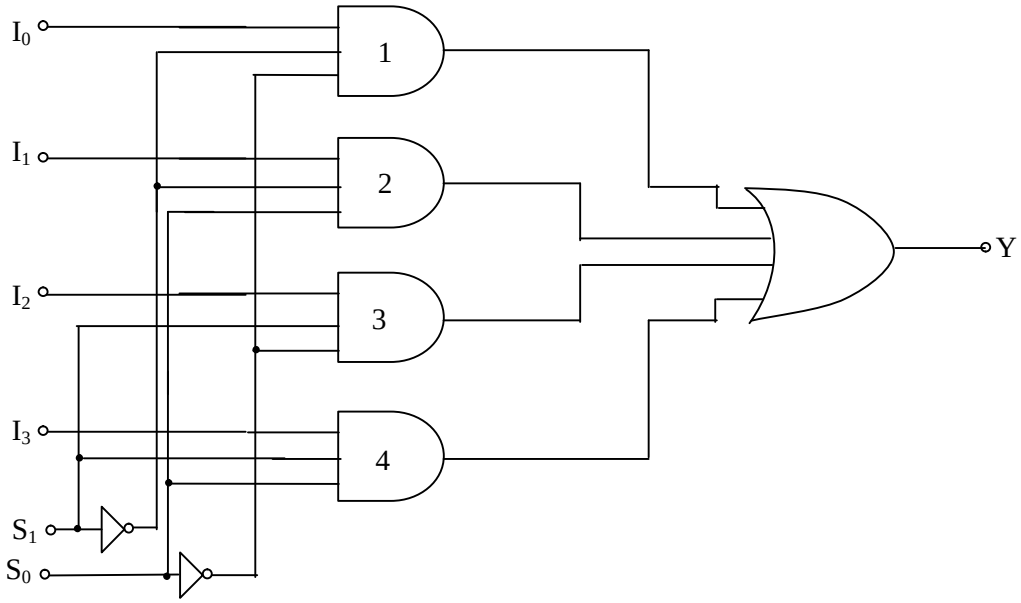
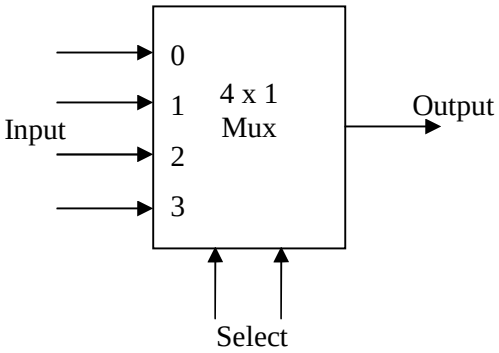


Fig (h): 4 to 1 Multiplexer

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Fig (i)



Fig(j)

Based on the combination of S_1 and S_0, the input associated with the selected AND gate finds out the path to reach the output through OR gate. For example: when $S_1S_0 = 01$, it selects the AND gate 2. So the input I_1 is transferred to the output i.e OR gate output is now equal to the value of I_1. thus providing a path from the selected input to the output. The remaining AND gates have at least one input equal to 0.

As in decoders, multiplexer IC have an enable input (or) storbe input to control the operation of the unit. It can also be used to expand two or more multiplexers to a digital multiplexer with a large number of inputs.

In data processing out of several types of circuits, multiplexer is one often used. The word" multiplex" means "many to one". A multiplexer circuit has many inputs but only one output. It takes several inputs from different channels but selects one out of these and feeds it to the output

TRUTH TABLES:

Multiplexer truth table

A	B	C	Y=AC+BC
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Decoder truth table

A	B	LD1	LD2	LD3	LD4
0	0	0	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	1	1	1	0

. Truth tables of different logic gates are to be verified.

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PRECAUTIONS:

1. The connections should be correct if any one of the connection is loose then it will give different out put.
2. The truth tables should be verified correctly
3 There should not be any of the basic connections

RESULT: Using NAND gate and NOT gate we can verify the truth tables of multiplexer and binary decoder.

A multiplexer can also be used to generate a desired logical function besides the selection of the channel and passing on to the output.